A Single-Phase Single Source Seven-Step Boost Inverter with Soft Charging of Switching Capacitors

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Abstract: The switching capacitor-based Multi-Step Inverter (MSI) has gained importance due to its boosting capability and self-balancing competency. Charging methodology is a key concern with the configurations of such capacitors. Charging of capacitors by pulsed current limits their application. The current paper introduces a soft-switching-based single-phase single-source, 7-Step (1S-7S) Multi-Step Boost Inverter (MSBI) to address the challenge of charging with better applicability. The proposed 1S-7S MSBI contains less number power devices and efficiently produces load with a voltage amplification ratio of three. The switching capacitor is charged using an inductor, which limits the pulsed current charging and ensures faster charging. This method of charging boosts the lifespan of the switching capacitor. The proposed topology is validated across various reference signals and load conditions in both simulation and laboratory settings. The results demonstrate the viability and reliability of configurations of MSI systems. The Total Harmonic Distortion (THD) of the output voltage and current are 15.01% and 2.52% in the simulation, and 17.28% and 3.89%, respectively, in the experimental results. Overall, the proposed system is found to be more advantageous in comparison to the existing topologies.

Keywords: Switching Capacitor, Self-balancing, Pulsed Charging, Soft Charging, Multi Step Inverter.

1. INTRODUCTION

Multi-Step/Level Inverters (MSI/MLI) have gained popularity in medium and high-voltage applications such as Flexible AC Transmission Systems (FACTS), traction drives, High-Voltage Direct Current (HVDC) systems, especially in renewable energy systems. Throughout the past few years, various MSI topologies have been devised and executed in commercial and industrial applications. The MSIs are of two types: symmetric and asymmetric, based on the DC source magnitude. Conventional MSIs face several challenges, such as a higher number of source requirements, balancing capacitor voltages, and the demand for large switches (Poorfakhraei et al., 2021; Jakhar et al, 2023; Peddapati and Kumar, 2023). To resolve these concerns, numerous papers have been published lately, primarily aimed at cutting down the switch count of MSI. The reduced MSI has advantages such as less electromagnetic interference, high reliability, reduced power switching elements, and reduced output voltage and THD with an increased number of output voltage steps.

The reduced switch types of MSI have several voltage amplification capabilities. Different types of MSIs such as Voltage Boosting SC-MSI (Peddapati et al., 2023), SC based 7L Boost MSI (Lin et al., 2021), Boost Active Neutral Point Clamped (NPC) with reduced switch count MSI (Baksi et al., 2023), Low Voltage stress 7L multi-step inverter based on SC (Zhao et al., 2021), A 7L with natural voltage balancing and boost capability (de Brito et al., 2022), 7L-T-Type SC MLI (Alyami et al.,2021), 7L-Triple Boost MSI (Srivastava and Seshadrinath, 2022)A 7L SC based MSI with modified PWM strategy (Mondal et al., 2024), 7L-Single Source MSI with triple boosting capability (Zaid et al.,2024), Transformer less 7L-Triple Boosting MSI (Kurdkandi et al., 2024), Single Phase SC based MSI interfacing with solar photovoltaic system(Sen et al., 2023), High step up SC-based MSI Topology (Shahsavar et al. , 2022), Quasi resonant SC based 7L multi-step inverters (Singh et al, 2022), A new boost type single source 7L SC MSI with reduced current stress(Marangalu et al., 2024), etc. are proposed in extant literature with different device counts, control techniques and modulation techniques to enhance the performance.

Most of the earlier studies on MSIs have focused on increasing the number of voltage steps in inverters by augmenting with additional Switching Capacitors (SCs) and power devices.

Peddapati and Kumar (2023) designed a circuit diagram that elevates the supply voltage to 1.5 times the input

level, where the SC unit generates various voltage steps. Some other topologies, as reported in (Lin et al., 2021; Zhao et al., 2021; Bakshi et al., 2023), incorporate voltage-escalation and auto-balancing SC features with a voltage lift of 1.5Vdc. A 7L SC-based MSI with natural voltage balancing (Alyami et al.,2021; de Brito Cardo et al., 2022) can produce a 7-step output with a maximum voltage lift of 1.5. In contrast, circuit configuration proposed earlier (Srivastava and Seshadrinath, 2022; Mondal et al., 2024; Zaid et al. 2024) can achieve a 7-step output with a voltage lift of 3. In traditional SC-based MSIs, self-adjusting voltage control involves parallel charging of SCs with the DC voltage source. This generates pulsed charging currents that are 5 to 6 times the current flowing through the load, which affects both reliability and practical implementation.

To address pulsed current issues and maintain the advantages of SC-based MSIs, recent research has focused on smoothly charging with SC-based MSIs. The topology proposed by (Shahsavar et al. 2022) can enhance the output voltage by three times, though it suffers from continuous charging of capacitor. This demands the use of a capacitor voltage balancing algorithm. Furthermore, the higher total voltage stress leads to a decrease in the efficiency of the MSI. The circuit proposed by (Singh et al.2022) has eleven devices and three reactive elements, which is of a higher count. Additionally, the capacitor used in this topology is intermittently charged, which requires six power devices to perform charging. This reduces the overall performance of the MSI. The methodology reported in (Maranagalu et al., 2024) employs a current-regulating circuit with a diode and an inductor but has six devices in the charging path of the capacitor. Moreover, this topology has two hefty capacitors to generate a 7L load voltage. Overall, smooth-charging SC-MSIs significantly improve upon traditional designs by mitigating pulsed charging currents and enhancing output voltage.

Yadav et al.(2019) described a seven-level inverter topology that adopts a hybrid design that integrates a five-level Neutral Point Clamped (NPC) inverter with a three-level T-type converter for induction motor drive applications. This topology necessitates additional capacitors, complicating the active balancing of floating capacitors and raising the computational demands on control algorithms. (Manoj et al. 2012) integrated two quasi-Z-source networks with a 7-level cascaded MLI, which can complicate the design. Additionally, the proposed modulation technique necessitates intricate control algorithms that require advanced expertise. A-NPC inverter is proposed in two earlier studies (Sathik et al., 2019; Lee et al., 2019). This topology requires an additional voltage balancing circuit, leading to an increased number of necessary power components. In (Ren et al., 2022), a hybrid cascaded multilevel inverter is introduced for its high-quality output, but controlling the input capacitor voltage is vital for normal operation, and varying load conditions can complicate this, necessitating effective control strategies for consistent performance and reliability. (Saleh 2023) proposed design of 7-level flying-capacitor (FC) inverters. This topology necessitates extra power switches, diodes, and capacitors. Balancing the voltages of the capacitors in these configurations poses a significant challenge. In another work (Saleh, 2022), a 7-level symmetric multilevel inverter is proposed. This inverter's configuration requires separate DC sources, thereby complicating the overall circuit structure significantly. The current study aims to advance the soft-charging concept to higher voltage levels. It proposes a 7-level capacitor-based topology that retains self-balancing and voltage-boosting features. In this work, a soft-switching-based single-phase single-source, 7-Step (1S-7S) multi-step boost inverter (MSBI) is proposed.

The key objectives of the proposed work are as follows:

- Design and develop a single-phase, single-source 7-step (1S-7S) multi-step boost inverter.
- Perform detailed analysis of the 1S-7S inverter using MATLAB/Simulink.
- Implement real-time experimentation with the DSP TMS320F28379D controller.
- Compare the performance of the 1S-7S inverter with other similar 7-step configurations.

The paper is presented in the following sections. Section 2 Proposed Single-Source Seven-Level Multilevel Inverter Topology, operation of 1S-7S MSBI and elaborates multi-carrier modulation scheme used to generate Pulse Width Modulation (PWM) signals for the proposed configuration. Section 3 covers the outcomes from simulated scenarios and practical implementations, Section 4 compares the proposed configuration with a similar configuration available in the literature, and the conclusion is elucidated in Section 5.

2. PROPOSED SINGLE SOURCE SEVEN LEVEL MULTILEVEL INVERTER TOPOLOGY

The single-phase 1S-7L Multilevel Inverter (MLI) model proposed is illustrated in Fig. 1. This design incorporates eight unidirectional switches (PD_1 to PD_8) that are responsible for adjusting load voltage levels. Furthermore, two complementary unidirectional switches (PD_{B1} and PD_{B2}) along with the inductor, L, are employed to facilitate the smooth charging of the capacitor, C. The topology shows a DC voltage source having a specific magnitude of V_1 and a capacitor with a magnitude of V_2. For this study, an asymmetrical configuration is adopted where $V_1 = V_{IN}$ and $V_2 = 3V_{IN}$

In conventional switching-capacitor-based topologies, the absence of an inductor can result in significant pulsed currents during the capacitor energy replenishment phase. The inclusion of a small inductor, however, minimizes these pulsed currents, as its losses are relatively negligible. The remaining switches in the system are arranged in a packed U cell pattern, which is necessary for generating multilevel voltage waveforms. This configuration allows for effective voltage level management while controlling ripples and maintaining efficiency.

2.1 Modes of Operation

Table 1 shows different switching modes of operations that generate various multilevel output voltages. In this table, a checkmark (✓) signifies that a power device is in the CONDUCTION state, and an "X" indicates the OFF state. This asymmetrical configuration generates seven

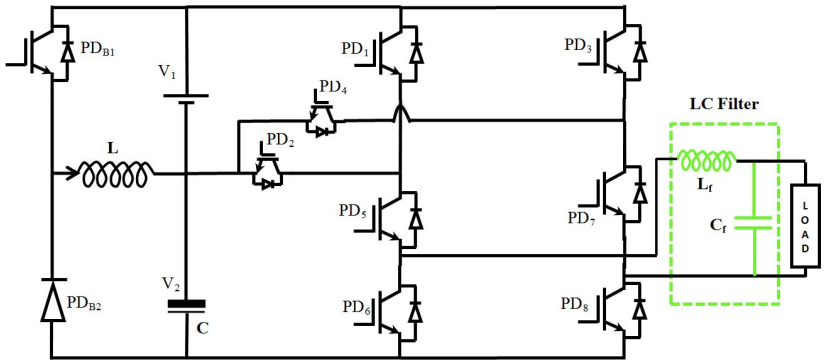

Fig. 1. Configuration of single phase 1S-7L MLI topology

Table 1. Switching States of Power Devices

Mode	PD_1	PD_2	PD_3	PD_4	PD_5	PD_6	PD_7	PD_8	V_{load}	Figure
State 1	✗	✗	✓	✗	✓	✗	✓	✗	$+3V_{in}$	2(a)
State 2	✗	✗	✓	✓	✓	✗	✓	✗	$+2V_{in}$	2(b)
State 3	✗	✓	✓	✓	✓	✗	✓	✗	$+V_{in}$	2(c)
State 4	✗	✓	✗	✗	✗	✓	✓	✓	0	2(g)
	✓	✓	✗	✗	✗	✓	✓	✓	0	2(h)
State 5	✓	✓	✗	✓	✗	✓	✗	✓	$-V_{in}$	2(d)
State 6	✓	✓	✗	✓	✗	✓	✗	✗	$-2V_{in}$	2(e)
State 7	✓	✓	✗	✓	✗	✗	✗	✗	$-3V_{in}$	2(f)

✓ Device On ✗ Device Off

output voltage levels, such as $+3V_{in}$, $+2V_{in}$, $+V_{in}$, 0, $\pm V_{in}$, $\pm 2V_{in}$, and $\pm 3V_{in}$. The multiple switching conditions and their corresponding voltage levels for the devised architecture are provided in Table 1 and depicted in Fig. 2.

The functionality of the proposed 1S-7S is analysed and illustrated in Fig. 2. The switches PD_{B1} and PD_{B2} are controlled with a duty cycle designed to adjust the charge on capacitor C so that its mean voltage is twice the DC input voltage, i.e., $V_2 = 2V_{IN}$. This asymmetrical charging setup enables the system to produce a seven-step (7S) load voltage, with a maximum voltage of $3V_{IN}$.

The switches S_{B1}, S_{B2}, inductor L, and capacitor C work according to the buck-boost principle. In it, these components operate independently of the rest of the circuit.

The switches S_{B1} and S_{B2} operate at a fixed switching frequency f_{switch} and a regulated duty cycle δ to guarantee desired capacitor voltage of $2V_{IN}$. During the inductor's charging phase, the current i_{ind} through the inductor increases linearly as shown in Fig. 3 and Fig. 4. The corresponding relationships are given in Equations (1) and (2) below:

$$V_{\text{ind}} = L\frac{di_{\text{ind}}}{dt} = V_{\text{in}} \tag{1}$$

$$i_{\text{ind}} = \frac{V_{\text{in}}\,\delta}{Lf_{\text{switch}}} \tag{2}$$

In the discharging period, the current through the inductor i_{ind} reduces linearly in accordance with the equations (3) and (4) shown below:

$$V_{\text{ind}} = L\frac{di_{\text{ind}}}{dt} = -V_{\text{cap}} \tag{3}$$

$$i_{\text{ind}} = \frac{V_{\text{cap}}(1-\delta)}{Lf_{\text{switch}}} \tag{4}$$

Equating equations (2) and (4) we derive relationship shown in equation(5):

$$V_{cap} = \frac{\delta V_{in}}{1-\delta} \tag{5}$$

To achieve capacitor voltage of $2V_{IN}$, δ should be set to 0.667, as outlined in equation(5).

The overall expense of power converter is heavily impacted by the stress induced by voltage and current levels experienced by different power devices. Hence, the proposed converter's voltage and current stress based on the input voltage and load current are analysed. Table 2 shows how power devices' voltage withstands and current-carrying abilities. PD_1 through PD_4 can withstand blocking voltages of V_{IN}. PD_5 and PD_7 are designed for $2V_{IN}$, and PD_6; PD_8, PD_{B1}, and PD_{B2}, support up to $3V_{IN}$. All devices are rated to carry the load current i_{load}, except PD_{B1}, and PD_{B2},, which are designed to handle current stress corresponding to the inductor current i_{ind}. The switching sequence and control timing were strategically optimized so that high-voltage handling devices operate at lower frequencies, thereby minimizing electrical stress across all power components.

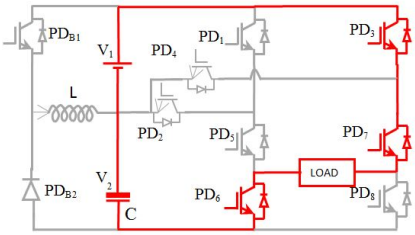

Fig. 2a. $V_{load} = 3V_{IN}$

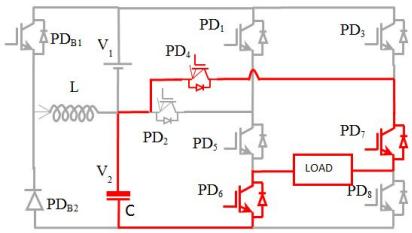

Fig. 2b. $V_{load} = 2V_{IN}$

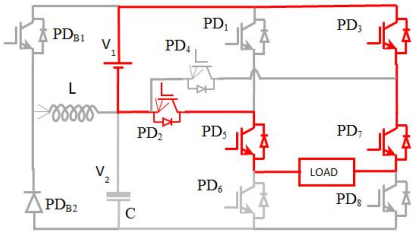

Fig. 2c. $V_{load} = V_{IN}$

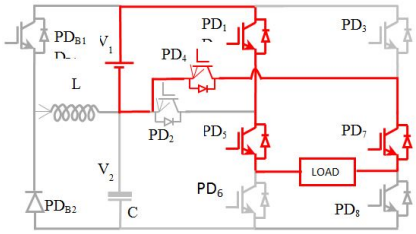

Fig. 2d. $V_{load} = -V_{IN}$

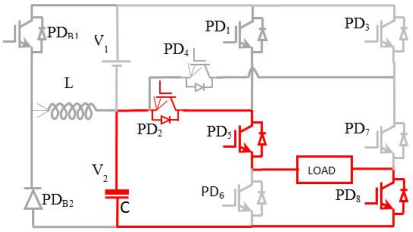

Fig. 2e. $V_{load} = -2V_{IN}$

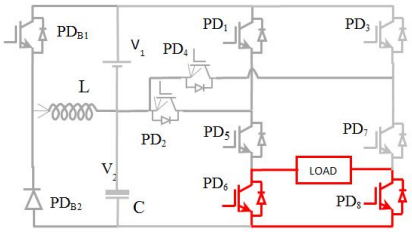

Fig. 2f. $V_{load} = -3V_{IN}$

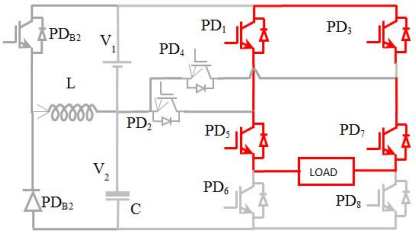

Fig. 2g. $V_{load} = 0$

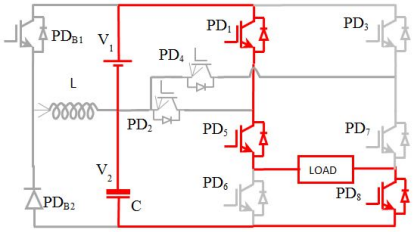

Fig. 2h. $V_{load} = 0$

Fig. 2. Load voltage output for different switching states

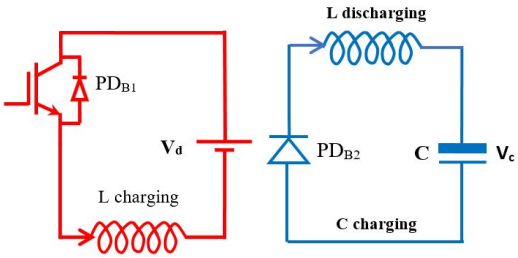

Fig. 3. Capacitor Charging Circuit

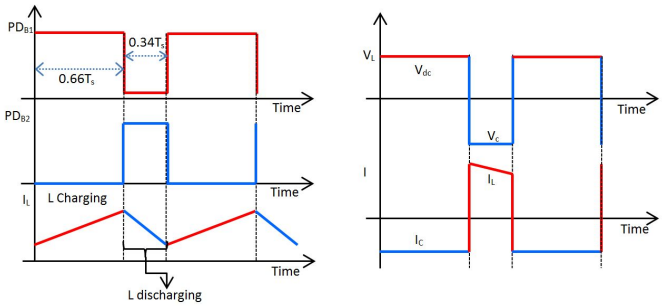

Fig. 4. Demonstrates the charging and discharging operation of the capacitor through the inductor

2.2 Multiple Carrier Modulation Scheme

The proposed converter uses Amplitude Shifted Carrier Wave (ASCW) modulation schemes to generate PWM

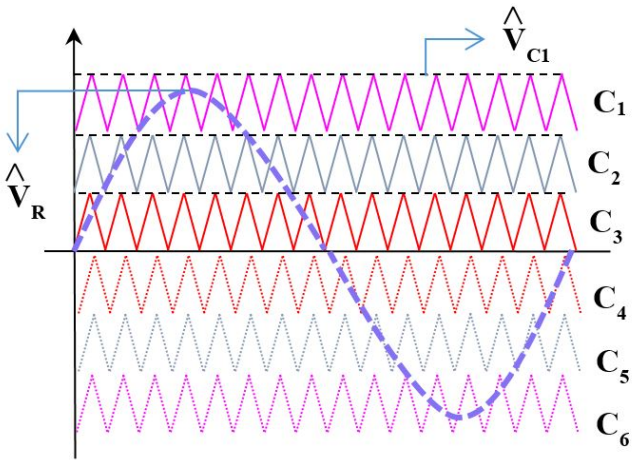

Fig. 5. Reference wave and carrier waves

pulses as represented in Fig. 5. The fundamental sine wave is juxtaposed with six high-frequency carrier waves. This comparison determines the state of operation of the converter as indicated in Table 1. Analyzing data on the state of operation, the PWM signals to the power devices are derived using MATLAB/Simulink software. The peak value of the fundamental load voltage is given by expression shown in equation(6):

$$\hat{V}_f = m_a \hat{V}_{load} \tag{6}$$

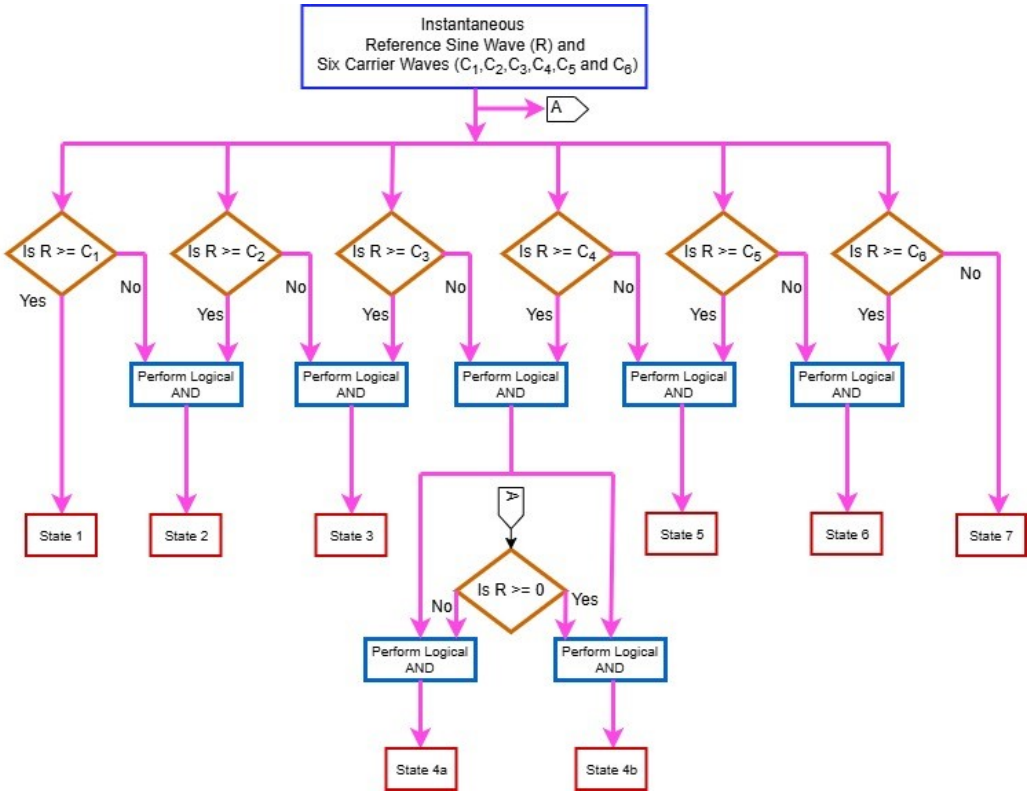

Fig. 6. Logical Flowchart for PWM generation.

where m_a denotes the amplitude modulation index which is denoted as $m_a = \frac{\hat{V}_R}{\hat{V}_{C1}}$ as indicated in Fig. 5. Fig. 6 shows the logical flowchart for generating switching signals for controlling the power devices.

3. EXPERIMENTS AND REFLECTIONS

3.1 Simulation Results

Initially, the proposed 1S-7S inverter is simulated using MATLAB/SIMULINK to validate its performance using a laboratory study. The proposed configuration is designed for a 500VA power rating with an input voltage of 100 Volts. Table 3 and 4 presents the electrical specifications used for the simulation and experimental study, along with the Bill of Materials (BOM) for the proposed multilevel inverter. The simulation results for the 1S-7S inverter with modulation index $m_a = 1$ are shown in Fig. 7(a-e) Output voltage has seven steps starting from 0 to ±100, ±200 and ±300.

Table 2. Power devices' voltage withstand and current-carrying abilities

Stress	PD_1 to PD_4	PD_5	PD_7	PD_6	PD_8	PD_{B1}	PD_{B2}
Voltage	V_{in}	$2V_{in}$			$3V_{in}$		
Current	i_{load}				i_{ind}		

Fig. 7 shows MATLAB/Simulink simulation results for load voltage, load current, and capacitor voltage of the proposed circuit. Fig. 7(a) shows the amplitude modulation index (ma) is set to 1 for an RL load of 20 ohms and 15 mH. In Fig. 7(b), while the ma remains at 1, the load transitions from resistive to RL in 0.4 seconds. The simulations shown in Fig. 7(c) and 7(d) resemble those conducted for Fig. 7(b), but with ma values decreased to 0.666 and 0.333, respectively, resulting in load voltage in 5 and 3 steps, respectively. Fig. 7(e) shows simulation results for ma=1 with Vin transition from 100V to 150V at 0.3 sec and load transitions from resistive to RL at 0.4 sec.

From the Fig. 7 (f), it is observed that the THD of the load current varies with the load, achieving a minimum value of 2.468% at a load resistance of 30 Ω. The current THD increases for both lighter and heavier loads, reaching 5.236% at 100 Ω and 4.439% at 10 Ω, indicating improved harmonic performance at moderate load conditions.

In the proposed MLI, a low-pass filter is connected at the load side, consisting of an inductor L and a capacitor C. (Hinago, Y., & Koizumi, H 2011). It is observed that the output voltage and current THD are reduced from 15.01% and 2.52% to 13.85% and 2.38%, respectively

3.2 Hardware Experimental Results

The introduced 1S-7S MLI was experimentally verified using a lab-scale prototype, as depicted in Fig. 9. A stabilized 100V DC power supply was utilized to energize the system. To generate the required control pulses, a Digital Signal Processor (DSP) TMS320F28379D controller (Texas Instruments Inc., Dallas, Texas, USA) was used. This level-shifted pulse-width modulation method was implemented. Gate signals for the power switches were generated using an opto-coupler-based driver circuit as shown in Fig. 8, specifically the TLP250H, which facilitated the formation of the desired output voltage waveform. The table .4 shows the scope parameters.

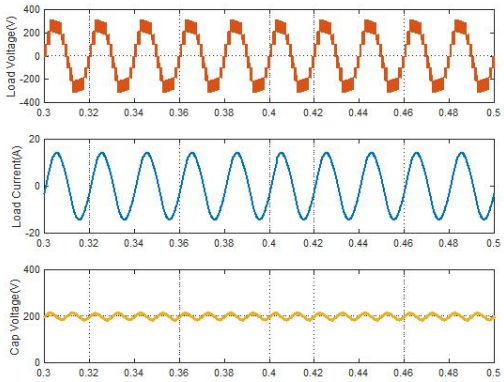

Fig. 7a. ma=1 with RL load

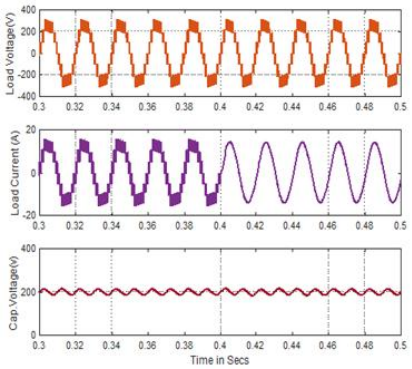

Fig. 7b. ma=1 with load transitions from resistive to RL at 0.4 seconds

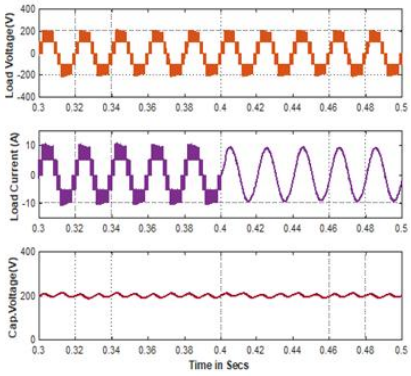

Fig. 7c. ma=0.666 with load transitions from resistive to RL at 0.4 seconds

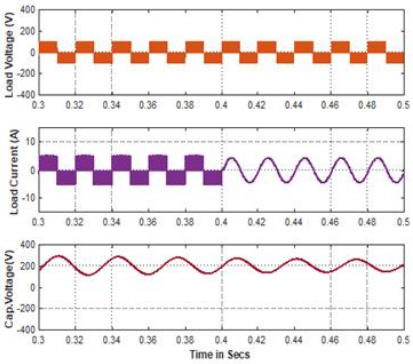

Fig. 7d. ma=0.333 with load transitions from resistive to RL at 0.4 seconds

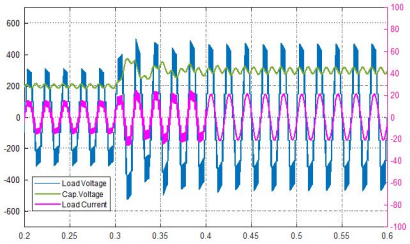

Fig. 7e. ma=1 with Vin transition from 100V to 150V at 0.3 secs and load transitions from resistive to RL at 0.4 seconds

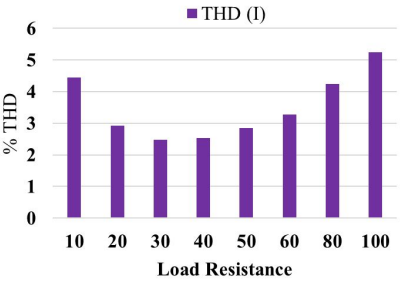

Fig. 7f. Load sensitivity analysis

Fig. 7. Simulation Results

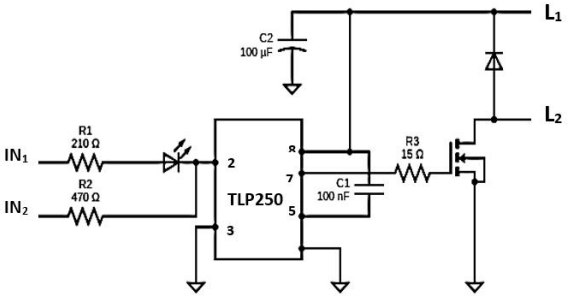

Fig. 8. Driver circuit for power switching devices

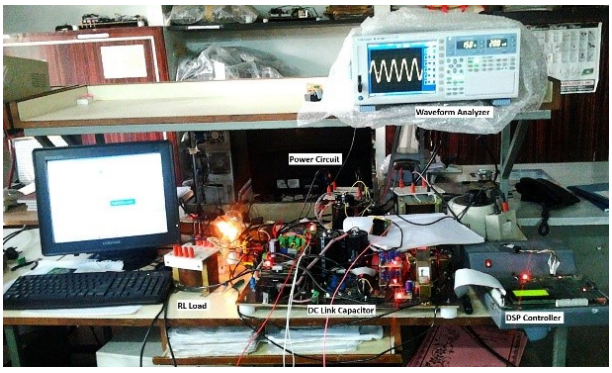

Fig. 9. Hardware setup of the proposed inverter

Table 3. Electrical specifications taken for the simulation and experimental study

Components	Specifications
Input voltage V_{in}	100 V
Reference frequency (f_r)	50 Hz
Switching frequency (f_s)	5 kHz
Load resistance and inductance	20 Ω and 15 mH
Soft charging inductor	3 mH / 5A - Ferrite core
DC link capacitor	1000 μF
Power Devices (PD1-PD4)	IRF610, 200V
Power Devices (PD5 & PD7)	IRFP4868PbF, 300V
Power Devices (PD6, PD8, PD_{B1}, PD_{B2})	IPW50R280CCE, 500V
Capacitor Type	ALC70 aluminum electrolytic / ESR-143 mΩ / 400V
Load Inductor	15 mH / 5A - Ferrite core
Heat sinks	TO-220

The static and dynamic behaviors of the proposed 7-level inverter are depicted in Fig. 10. Fig. 10(a) presents the steady-state output voltage with a load of 20 Ω. Fig. 10 (b) shows fundamental and harmonic values in the voltage. The load voltage waveform has a THD of 4.483%. The load voltage and current waveforms of the proposed 1S–7S

Table 4. Electrical specifications optocoupler

Components	Specifications
Opto coupler	TLP250H
Gate Resistance	15 Ω, 0.25 W
Input Resistance R1	470 Ω, 0.25 W
Input Resistance R2	210 Ω, 0.25 W
Compensating Capacitor	100 nF / 25 V (ceramic)
Decoupling Capacitor	100 μF / 25 V (ceramic)

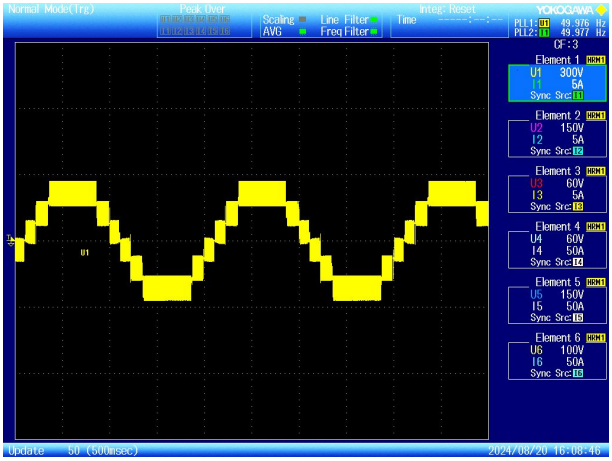

Fig. 10a. Steady state output voltage waveform of the proposed 1S-7S inverter

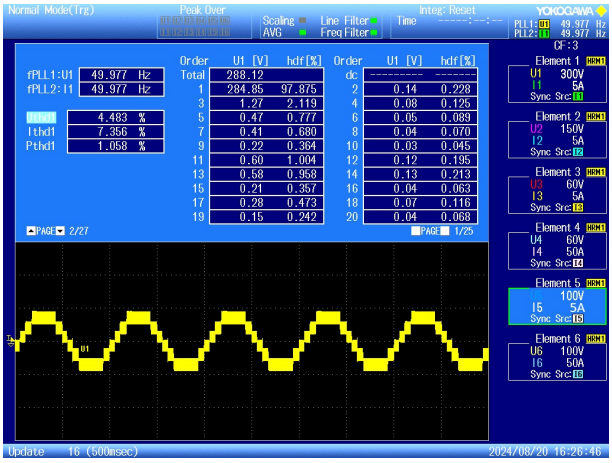

Fig. 10b. Fundamental and harmonic content in the load voltage of the proposed inverter

inverter are shown in Figure 10(c) for a resistive–inductive (RL) load with a resistance of 20 Ω and an inductance of 30 mH, respectively. The inverter's dynamic response is depicted in Fig. 10(d) and 10(e). Fig. 10(d) shows that load varies with a decreasing power factor, starting from Z1 = 20 Ω, then changing to Z_1 = 20 Ω + 300 mH, and finally to Z_2 = 40 Ω + 150 mH. Fig. 10(e) captures the waveforms of output voltage, current, and voltage across the capacitor during abrupt load transition conditions. In both scenarios, the inverter successfully maintains the load voltage at the desired level, thereby demonstrating stable performance under dynamic load conditions.

4. TOPOLOGY COMPARISONS

To illustrate the performance of the proposed converter, a meticulous assessment of differences is conducted between

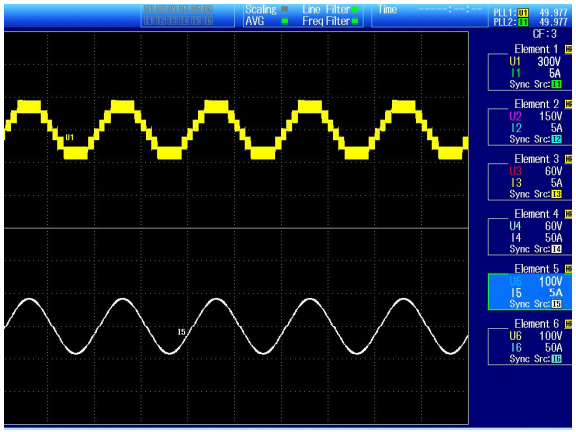

Fig. 10c. Load voltage and current waveform for RL load

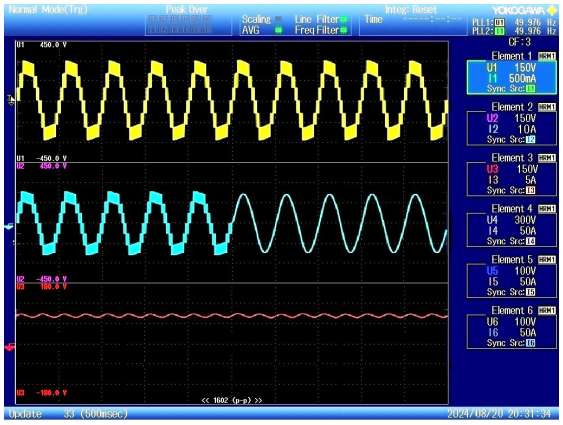

Fig. 10d. Load Voltage, Current and capacitor voltage waveform during load shifting from R to RL.

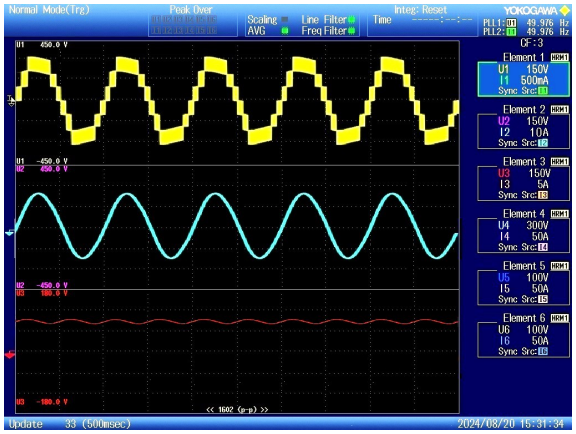

Fig. 10e. Load voltage, current and capacitor voltage waveform for RL load

the proposed converter with the conventional converters and recent published converters on switching capacitor-based multi-step converters as detailed in Table 5 and illustrated in Fig. 11.

Voltage Step to Device Count Ratio(VSDC) and Total Voltage Induced Stress (TSV) on Switching Devices are calculated based on equations (7) and (8), as shown in Table 5.

$$V_{SDC} = \frac{\text{Number of Steps in Load Voltage}}{N_{CPD} + N_{CBPD} + N_{UCPD}} \qquad (7)$$

Table 5. Comparison of Reported Multilevel Topologies

Ref.	N_{CPD}	N_{CBPD}	N_{UCPD}	N_r		N_{PDRP}	I_{MS}	VSDC	VAR	TSV	$\frac{TSV}{VAR}$	Soft charging	Continuous charging
				Cap.	Ind.								
(Peddapati, S. and Kumar, B., 2023)	9	–	–	2	–	3	$I_L + I_C$	0.77	1.5	7.5	5	✗	✗
(Lin et al., 2021)	7	–	2	2	–	3	$I_L + I_C$	0.77	1.5	6.5	4.3	✗	✗
(Baksi, S.K. and Behera, R.K., 2023)	6	2	–	3	–	4	$I_L + I_C$	0.875	1.5	13	8.6	✗	✗
(Zhao et al., 2021)	6	2	–	2	–	4	$I_L + I_C$	0.875	1.5	8	5.3	✗	✗
(de Brito Cardoso et al., 2022)	10	–	2	3	–	4	$I_L + I_C$	0.58	1.5	11.3	7.5	✗	✗
(Alyami et al., 2021)	7	1	–	2	–	4	$I_L + I_C$	0.875	1.5	6.5	4.3	✗	✗
(Srivastava, A. and Seshadrinath, J., 2022)	7	1	2	3	–	5	$I_L + I_C$	0.7	3	27	9	✗	✗
(Mondal et al., 2024)	10	–	2	–	4	4	$I_L + I_C$	0.7	3	21	7	✗	✗
(Zaid et al., 2024)	10	1	2	3	–	3	$I_L + I_C$	0.636	3	21	7	✗	✗
(Kurdkandi et al., 2024)	8	–	2	3	–	3	$I_L + I_C$	0.7	3	21	7	✗	✗
(Sen, P et al., 2023)	8	–	2	3	–	4	$I_L + I_C$	0.7	3	16	5.3	✗	✗
(Shahsavar et al., 2022)	8	1	1	1	2	2	I_L	0.7	3	22	7.3	✓	✗
(Singh et al., 2022)	10	1	2	1	6	6	I_L	0.636	3	16	5.3	✓	✗
(Marangalu et al., 2024)	9	–	2	2	1	6	I_L	0.636	3	22	7.33	✓	✓
1S-7S	9	1	–	1	1	Nil	I_L	0.7	3	20	6.66	✓	✓

N_{CPD}: No. of controlled power devices
N_{UCPD}: No. of uncontrolled power devices
N_r: No. of reactive elements
N_{PDRP}: No. of power devices in reactive elements path
I_{MS}: Max current stress
I_L: Load current
I_C: Charging current
VSDC: Voltage Step to device count ratio
VAR: Voltage amplification ratio
TSV: Total voltage induced stress on switching devices
N_{CBPD}: No. of controlled bidirectional power devices

$$TSV = \sum_{i=1}^{N_{CPD}+N_{UCPD}+N_{CBPD}} V_{PD(i)} \tag{8}$$

where $V_{PD(i)}$ denotes the voltage withstanding capability of the ith power device.

Table 6. Measurement setup parameters

Components	**Specifications**
Scope Model	Yokogawa WT1800 Power analyzer
Bandwidth	5 MHz
Current probe	701928 – 100 MHz, 30 ARMS
THD method	FFT window
Dead Time	10 μs

As shown in Table 5, the majority of the converters do not support soft charging. Among the aggressively charged 7S topologies, the one proposed by (Peddapati 2023) requires only six gate drivers, the lowest count compared to other topologies. However, it falls short in terms of voltage amplification capability. The number of capacitors shown in (Lin, et al., 2021) is four (maximum) when compared with other configurations. Hence, the circuit becomes hefty. Moreover, some circuit configurations as reported earlier (Lin et al., 2021; Zhao et al., 2021; de Brito Cardoso et al., 2022; Baksi et al., 2023;) have a voltage amplification factor equal to 1.5. Furthermore, the issue of pulsed charging impacting practical viability has not been addressed, which is also true for other aggressively-charging configurations. Some configurations proposed earlier have a voltage amplification factor equal

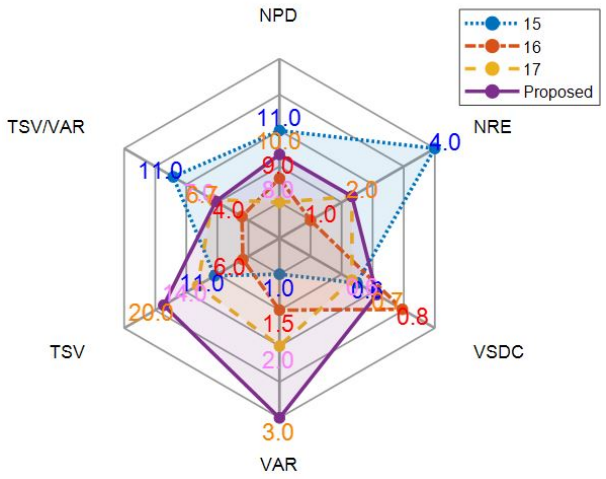

Fig. 11. Comparison between the proposed 1S-7S inverter with other similar topologies

to 3 and low VSDC, but again, those configurations could not apply soft charging techniques for capacitors.

To address the aforementioned issues, a few soft charging switch capacitors and multi-step inverters were proposed above. The circuit configuration proposed in (Singh et al, 2021) uses one dedicated inductor for soft charging, and it has a lower VSDC. However, it does not have voltage amplification ability. The circuit topology proposed by (Maranagalu et al. 2024) has slightly higher VSDC compared to that reported by (Singh et al.2022) and is also capable of amplifying the input voltage by 1.5 times. But topology reported by (Marangalau et al. 2024) requires sensing the voltage to maintain the voltage across the switching capacitors, which increases the cost of the topology. The circuit configuration proposed by (Yadav et al. 2019) has a lower VSDC and a voltage amplification factor of 2 and this configuration has a higher TSV and is capable of generating only five steps at the load voltage.

Notably, this proposed configuration is very effective in alternative energy systems with lower input voltage, because it constantly charges the capacitor from the DC supply while providing power to the loads and does not require a pre-charging setup.

5. INVERTER LOSSES AND EFFICIENCY CALCULATIONS

To determine the efficiency and analyse the breakdown of losses in the proposed 7-step inverter, power losses associated with its components are calculated. These losses are categorized into two main types: dynamic losses (those related to switching) and on-state losses (those related to conduction). The switching losses account for energy dissipated during the activation and deactivation of the switches, while conduction losses arise when the switches are in an active state. Additionally, the capacitors and inductors also contribute to losses due to current flow.

5.1 ON-State Losses

On-state losses occur because of various influences associated with the operation of power devices and passive elements in the configuration. These influences include the resistance faced while the devices are conducting (R_{DS-ON}), the equivalent series resistance linked to capacitors (ESR_C), and the inherent resistance present in inductors (ESR_L). The losses are computed by analysing these factors,

$$P_{\text{ON-STATE}\,(PD1-PD8)} = \frac{4}{\pi}\left[\int_0^{2\pi} R_{DS-ON}\, i^2_{load}(t)\; d(\omega t)\right] \tag{9}$$

$$P_{\text{ON-STATE}\,(SB1-SB2)} = \frac{1}{\pi}\left[\int_0^{2\pi} R_{DS-ON}\, i^2_{ind}(t)\; d(\omega t)\right] \tag{10}$$

$$P_{\text{ON-STATE Ind}} = \frac{1}{2\pi}\left[\int_0^{2\pi} ESR_L\, i^2_{ind}(t)\; d(\omega t)\right] \tag{11}$$

$$P_{\text{ON-STATE Cap}} = \frac{1}{2\pi}\left[\int_0^{2\pi} ESR_C\, i^2_{load}(t)\; d(\omega t)\right] \tag{12}$$

$$\begin{aligned} P_{\text{ON-STATE (Total)}} = {} & P_{\text{ON-STATE (PD1–PD8)}} \\ & + P_{\text{ON-STATE (SB1–SB2)}} \\ & + P_{\text{ON-STATE (ind)}} \\ & + P_{\text{ON-STATE (Cap)}} \end{aligned} \tag{13}$$

5.2 Dynamic Losses

The dynamic or switching losses in the circuit comprise the thermal power dissipated during both the activation (turn-on) and deactivation (turn-off) phases of the switches. To simplify the evaluation, the voltage across the switches and the current flowing through them are approximated using linear models. Consequently, the losses incurred during the switch-on and switch-off periods of each switch can be determined accordingly, as shown in equations (14) and (15) below:

$$\begin{aligned} P_{\text{Turn-ON}} &= \frac{1}{T_S}\left[\int_0^{T_{ON}} v_{PD(ON)}(t)\, i_{PD}(t)\, d(t)\right] \\ &= \frac{N_{ON} T_{ON}}{6}\, F_S\, V_{PD(ON)}\, I_{PD} \end{aligned} \tag{14}$$

$$\begin{aligned} P_{\text{Turn-OFF}} &= \frac{1}{T_S}\left[\int_0^{T_{OFF}} v_{PD(OFF)}(t)\, i'_{PD}(t)\, d(t)\right] \\ &= \frac{N_{OFF} T_{OFF}}{6}\, F_S\, V_{PD(OFF)}\, i'_{PD} \end{aligned} \tag{15}$$

where I_{PD} and I'_{PD} represent the current flowing through each switch immediately after activation and just prior to deactivation, respectively. N_{ON} and N_{OFF} correspond to the number of switch activations and deactivations within one complete switching cycle. T_{ON} refers to the combined duration of the turn-on delay and rise time, while T_{OFF} represents the total of the turn-off delay and fall time. These T_{ON} and T_{OFF} values can be obtained from the data sheets of the power devices used in the specified

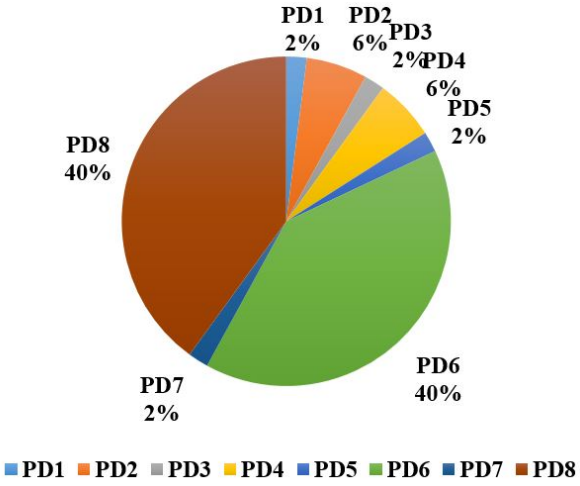

Fig. 12. Losses incurred by power devices

inverter. Furthermore, T_s and F_s denote the inverter's cycle duration and switching rate, respectively. The total switching losses for the inverter are then calculated as shown in equation(16):

$$P_{\text{Dynamic Losses (Total)}} = \sum_{j=1}^{10} P_{\text{Turn-ON}}(j) + P_{\text{Turn-OFF}}(j) \tag{16}$$

Therefore, total losses in the inverter and inverter efficiency can be determined as under using equations (13) and (16).

$$P_{TOTAL} = P_{\text{ON-STATE (Total)}} + P_{\text{Dynamic Losses (Total)}} \tag{17}$$

$$\eta = \frac{P_{OUT(\text{Inverter})}}{P_{OUT(\text{Inverter})} + P_{TOTAL}} \tag{18}$$

The Fig. 12 depicts the Conduction losses for each switch.

The total losses of various switches in the proposed seven-step inverter were calculated and are presented in Fig 12. The analysis reveals that higher losses occur between switching points PD6 and PD8, mainly due to increased current stress and switching frequency in these regions, which significantly influence the inverter's overall efficiency. The conduction losses in the IGBT and freewheeling diode are calculated as the product of the current flowing through the collector or anode and the corresponding saturation (on-state) voltage during the conduction period.

The efficiency of the proposed inverter at different output power levels is shown in Fig. 13. The results show that a maximum efficiency of 93.26% was observed at 5200 W.

5.3 Snubber Circuit Design For Power Device

A Snubber circuit is designed to protect fast switching devices by supressing voltage spikes that occur during switching transients as shown in Fig 14. It helps reduce

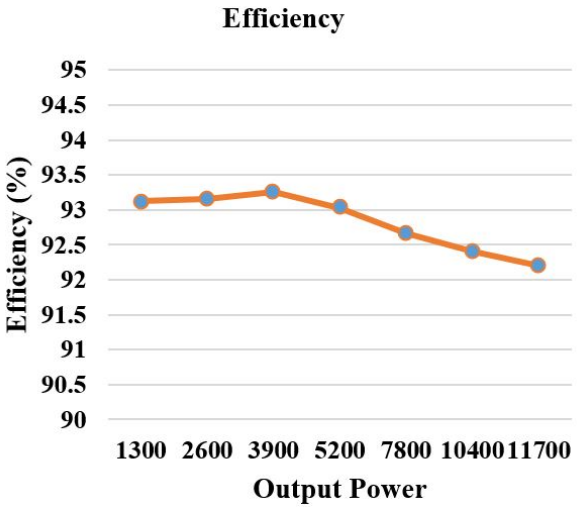

Fig. 13. Efficiency of proposed Multilevel inverter versus output power

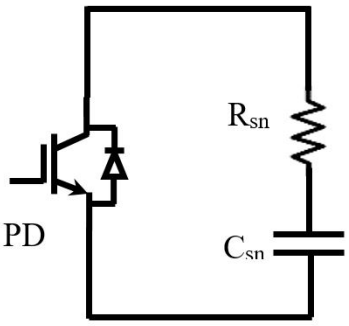

Fig. 14. Snubber circuit for power switches

stress during both turn-on and turn-off periods. (Zhang, Yi et al., 1995). The value of Snubber capacitance and resistance can be found using the equations (19) and (20).

Snubber Capacitance (Csn)

$$C_{sn} = \frac{L_s I_o^2}{V_{pk}^2 - V_{cc}^2} \tag{19}$$

Exact resistor value for full discharge in one period (Rsn):

$$R_{sn} = \frac{1}{(6 \cdot C_{sn} \cdot F_{sw})} \tag{20}$$

The equation (21) shows the average power dissipated in snubber resistor (Pr). Average power dissipated in snubber resistor (Pr):

$$P_r = \frac{1}{2} C_{sn}(V_{pk}^2 - V_{cc}^2) \quad \cdot F_{sw} \tag{21}$$

In designing the snubber circuit, the resistance and capacitance values are selected based on the operating conditions to ensure effective energy absorption and dissipation.

6. CONCLUSION

In this paper, a 1S-7S boost-type multi-step inverter is proposed. The proposed design shows notable advance-

ments over the existing switching capacitor-based multistep inverters, including enhanced soft-charging potential, uninterrupted capacitor charging, an increased number of voltage steps with fewer components, a higher voltage amplification ratio of 3, and minimized pulsed current. These features render the proposed inverter suitable for inverting applications. Testing under a range of circumstances has validated the practicality and performance of this proposed configuration. The output current THD is 3.89%, fulfilling the requirements of the IEEE-519 standard. With its numerous advantages, this configuration is an excellent choice for high-power quality and high-gain DC-to-AC conversion, particularly in grid-tied solar energy systems and similar applications.

DECLARATION
The authors declare no potential conflicts of interest and no funding is obtained to carry out this work.

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