Performance Analysis of Front-end Push-Pull Converter in a Single-Phase Inverter for Battery Current Ripple Reduction

R. Jeyaraman[1*], C. N. Ravi[2]

[1]Sathyabama Institute of Science and Technology, Chennai, Tamil Nadu, India.*
[1]Email: jeyam.apk@gmail.com*
[2]Vidya Jyothi Institute of Technology, Hyderabad, Telangana State, India.
[2]Email: dr.ravicn@gmail.com

Abstract: A two-stage inverter (TSI) produces high second-order ripples in the low DC battery voltage operation, which cannot be used in telecommunication applications. Furthermore, it reduces the battery's performance and lifespan. This work analyses dual closed-loop feedback in a push-pull converter for eliminating second-order harmonics at the input of a TSI inverter system. During the discharge of a battery, its voltage decreases while the DC-DC converter's pulse width modulation duty cycle approaches its maximum value. This creates an open loop in the existing closed-loop scheme that returns the second-order ripple at the battery input current. Introducing a battery voltage compensation stage in the existing system helps sustain the closed loop at a minimum operating voltage of the converter and maintains acceptable ripple levels. The proposed technique provides a viable solution for keeping the second-order ripple level at the entire operating range of the TSI inverter, even when the battery voltage decreases during discharge. Using the PSIM simulation tool, the proposed solution was validated in a push-pull converter, and the percentage of battery input current ripple was compared with the existing and proposed closed-loop control strategy. Finally, an 800 W/ 1 KVA prototype is built and tested, and the experimental results show that the proposed control techniques work to reduce ripples. The proposed control strategy has reduced the ripples from 10.2% to 1.4% at minimum operating voltage.

Keywords: Two-stage inverter (TSI), Dual closed-loop, DC-DC converter, Second order ripple, Push-pull converter

1. INTRODUCTION

The inverter is a device that converts DC power from stored batteries to AC power for critical power backup applications. Among the many application sectors of the inverter, telecommunication is one of the major sectors for power backup applications. In most cases, the inverter's backup input source is a battery; however, the new hybrid inverter can also work with a renewable energy source, such as a fuel cell (Dixit and Rashmi, 2015) or a solar cell (Jain and Agarwal, 2007). The TSI topology has been designed with two converters, a DC-DC converter and a DC-AC inverter. In the DC-to-AC power conversion process, the DC input power is used in a sinusoidal pattern, causing a ripple (Yang et al., 2019) at the DC input. The ripple frequency is related to the AC output power's fundamental frequency. This is a second-order value of the fundamental frequency propagating from the alternating current output to the DC input. It needs a large amount of LC filtering to stop passing this second-order harmonic to the DC input, and it is difficult to resist the passage of ripple to the front end of the DC-DC converter.

As a result, the battery current of the inverter exhibits a second-order sinusoidal ripple (O'Connor et al., 2021), affecting the battery's electrochemical process and reducing the battery's performance and life (Jung and Kim, 2014). Several research studies have done experiments to lower the ripple in the AC power using different techniques. To reduce (Zhang et al., 2017) proposed a model for reducing the ripple current using a full bridge inverter and boost converter in a TSI. The step-by-step approach allowed them to avoid errors while designing the system, producing improved performance and reducing the second harmonic current (Jung and Kim, 2014; Deng et al., 2016; Shi et al., 2015; Lu et al., 2017). The authors improved output ripple reduction in single-phase inverter systems using PI controllers for energy-storing systems (Ale and Abrishamifar, 2012; Shi et al., 2018; Xu and Ji, 2016). The research studies should be discussed about the broad operation range of the converter, and investigations are not considered isolated converter topologies. The telecom application inverters must have galvanic isolation between the safe, low voltage (48 V) and the hazardous high voltage (230 V). To satisfy industrial safety regulations, an isolated converter is introduced at the front end of the DC-DC stage to fulfil industrial safety standards and provide galvanic isolation between low voltage and hazardous voltage (Lee et al., 2011). On the other hand, the inverter battery ripple frequency is in the audible spectrum and injects a humming noise and inferences into the telecommunications system. The European telecom standards specifications specify low-frequency spectrum limits for the DC input ripple voltage (Jeyaraman and Ravi, 2020). Additionally, the manufacturers specify the acceptable percentage of ripple current limits. To meet the standard requirement, the isolated push-pull converter is used along with an active closed-loop ripple reduction system, which helps to cut down on second-order ripple at the input. This ripple reduction scheme has operated with two feedbacks taken from the DC-DC converter intermediate stage voltage and current. The typical telecom

inverter working voltage range is from 42 to 60 V, and at the nominal operating voltage, the dual closed-loop system controls the input current ripple well. While reducing the input voltage to a minimum, the dual loop system becomes an open loop, and a ripple appears in the battery current. The proposed research aims to reduce the ripple of the entire operating range of the inverter. The paper has validated the novel solution at the prototype level, and this article has investigated further the closed-loop control transfer function and system stability analysis of load impact and different types of load conditions. It has been validated in the real-time prototype inverter, ensuring the proposed novel solution makes a closed-loop and stable system. The balance of the article is structured as follows: The two-stage inverter's operating concept and existing dual closed-loop scheme control strategy are described in Section 2. Section 3 describes the proposed control strategy in a two-stage inverter, and the proposed closed-loop transfer function is derived and discussed. Section 4 presents the converter design considerations and analysis, such as the described transformer, input, and output filter designs. The experimental prototype's construction, design parameters, and test setup details are shown in Section 5. The converter performance, power loss, thermal analysis, and prototype converter stability validation results are presented in Section 6. The second-order ripple of the converter is compared between existing and proposed system simulations and experimental results. System efficiency and ripple analysis for the whole converter working range are also discussed. Suggestions for control strategies are also discussed. Finally, Section 8 concludes.

2. TOPOLOGY

2.1 TSI Topology with Front-end Push-Pull Converter

In this study, the TSI inverter was designed with a front-end push-pull converter. The push-pull converter (Ivanovic and Knezic, 2022) operation belongs to the buck converter theory. When the switch is ON, energy transfers to the load. The battery is connected through an input LC filter L_{In} and C_{In}. The Push-pull converter comprises two MOSFET Q_1 and Q_2 components that can be driven with a simple driver circuit that aids in the execution of complementary triggering operations. The push-pull transformer has two primary windings that help transfer energy on both operation cycles, and it also provides isolation between low-voltage and high-voltage circuits. To balance flux in the transformer, the primary is to be wound by bifilar winding. It helps avoid the possibility of core saturation and ensures good core utilization. Selecting a power transformer core and conductors suitable for the application is essential to ensure the highest possible efficiency. The TSI topology using the push-pull converter is depicted in Fig. 1.

The voltage gains of the push-pull converter (Musarrat et al., 2021) is given by (1)

$$U_{Int} = \left(\frac{N_S}{N_p}\right) U_{in} \times d - (2U_{diode} + U_{L1}) \quad (1)$$

In the above equation (8), U_{int} is the intermediate DC-link voltage, U_{in} is the DC input voltage from the battery, $N_p$and $N_s$are the primary and secondary number of turns of the transformer respectively, d is the duty cycle of the PWM, U_{diode} is the diode voltage drop (D1, D2, D3, D4), U_{L1} is the L_1 inductor voltage drop.

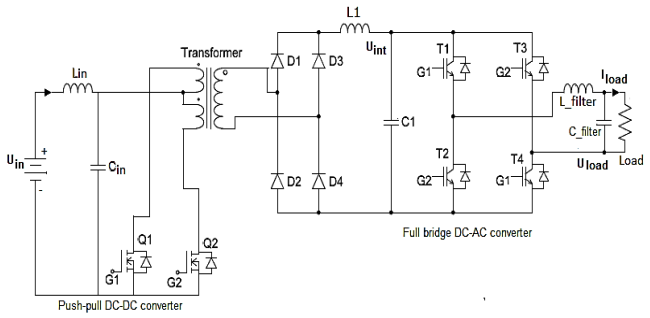

Fig. 1. The two-stage inverter with front-end push-pull converter.

The inverter section comprises four IGBTs (T1, T2, T3 and T4). Using sine pulse width modulation techniques (PWM), a full bridge inverter converts the DC-link voltage to an AC supply. Here, the DC power is transferred to a sinusoidal pattern and supplied to the load. As a result, the DC-link stage has a second-order ripple in the voltage and current. The DC link section has a passive filter of LC filter L_1 and C_1that plays a significant role in the ripple reduction (Musarrat et al., 2021; Ramakrishnan and Ravi, 2022). The C_1capacitor acts as a bank of energy storage and supports suppressing ripple from the load. Here, the second-order ripple propagates from the inverter output to the converter input. Using the active ripple reduction techniques, the input DC ripple was reduced.

2.2 Existing dual closed-loop Control Strategy

The active ripple reduction scheme is a dual closed-loop control system. This has two PI loops cascaded with voltage and current feedback. This would help to regulate the converter power. The push-pull converter triggering pulses are generated from the dual closed loop scheme. The control block diagram of the existing method is depicted in Fig. 2.

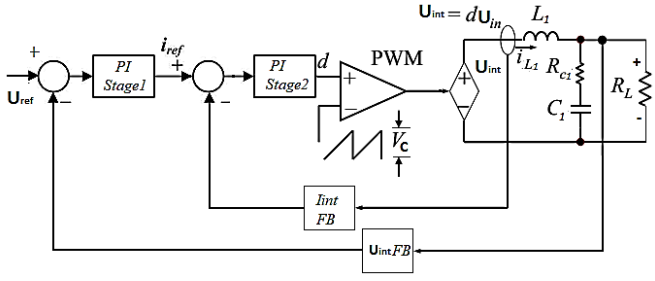

Fig. 2. The existing dual closed loop with fixed U_{ref}.

In the dual closed-loop control strategies, the DC-link section U_{int} and I_{int} are sensed to control the low-frequency DC ripple at the front end of the converter. The PI stage 1 set point is a U_{ref}fixed reference in the existing method. The fixed set point and U_{int} DC-link voltage feedback are compared and given to PI stage 1, which generates a current set point for the second closed loop. Likewise, the I_{int} set point from the converter output is compared to the PI stage 1 output, resulting in a PWM reference signal to the comparator. Here, the push-pull converter operates less than

0.5 duty cycle. Based on the input operating voltage and load, the converter pulse width is regulated and meets the closed loop set point. The ripple optimization was achieved with voltage and current loop regulation offset in the converter PWM duty cycle. When a converter's input voltage reduces, the PWM duty cycle reaches its maximum value, and there is no possibility of an offset for ripple control. This leads to a situation in which the cascaded PI loops, the voltage control loop becomes open, and the existing closed-loop control system doesn't control the ripple at the DC input source end. The PI stage1 has no regulation in the U_{int}voltage, the ripple reduction control system fails, and ripples exist at the inverter input current. The telecom inverter, the existing dual closed control system, has been unable to operate in the lower operating range (Jeyaraman and Ravi, 2020).

3. PROPOSED CONTROL STRATEGY IN THE TSI TOPOLOGY

The proposed method would add an adaptive voltage reference to the existing dual closed-loop scheme. The PI stage 1 fixed reference input is modified during the minimal operation range of the converter by introducing DC input source voltage sensing. To ensure consistent operation, a new control system is required better to manage ripple voltages at the DC input source end. The proposed solution has created modelling with the help of the PSIM simulation tool, which is the best tool for analyzing the converter ripple response in a closed-loop operation. The proposed closed-loop front-end push-pull converter is depicted in Fig. 3.

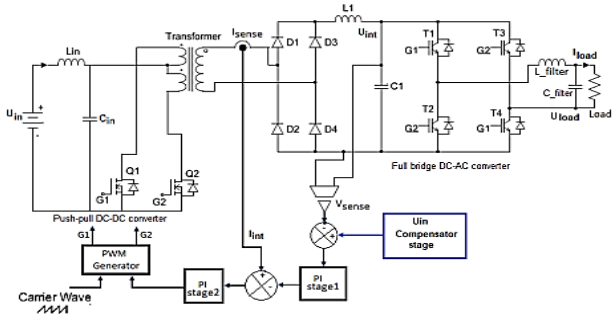

Fig. 3. The block diagram of the TSI Inverter with proposed closed loop.

In the proposed method, the U_{int} set point reference is defined by U_{in} from the battery voltage. The PI stage 1 voltage reference is derived from the battery U_{in} compensation stage. During the battery discharge operation, the U_{in} feedback to the compensation section reduces the voltage set point to the PI stage 1 reference. This gradually decreases the DC-link voltage and maintains the closed loop for the PI stage. The dual continuous feedback system controls the second-order ripple for the DC input. The proposed closed-loop scheme is depicted in Fig. 4.

The control block diagram of a proposed method is shown in Fig. 5. Where F_m, H_i and H_v are the PWM regulator gain, the current of the inductor feedback factor and DC-link voltage feedback factor, respectively.

Equation (11) describes the transfer function of the PI stage voltage loop, and equation (12) is also used to describe the transfer function of the PI stage current loop.

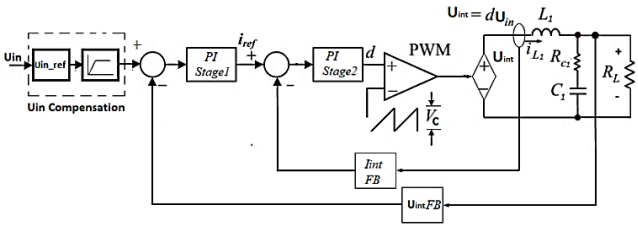

Fig. 1. The proposed closed loop with Uin compensation.

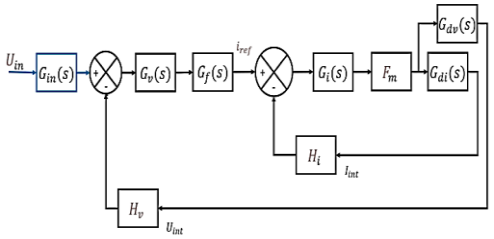

Fig. 5. The proposed closed-loop model.

The transfer function of the $G_{dv}(s)$ is given in equation (2),

$$G_{dv}(s) = \frac{R_L U_{in}}{L_{int}C_{int}R_L s^2 + L_{int}s + R_L} \quad (2)$$

The transfer function of the $G_{di}(s)$ is given in equation (3),

$$G_{di}(s) = \frac{(R_L C_{int}\, s+1)U_{in}}{L_{int}C_{int}R_L s^2 + L_{int}s + R_L} \quad (3)$$

The gain of the second loop is given by

$$T_i(s) = F_m\, H_i G_i(s)\, G_{di}(s) \quad (4)$$

When the loop is closed, the gain of the voltage loop, as given by

$$T_v(s) = \frac{G_v(s)G_i(s)F_m\, H_v G_{dv}(s) G_f(s)}{1+T_i(s)} \quad (5)$$

The dual-loop control theory (Wei et al., 2012; Shi et al., 2018) suggests that the cut-off frequency of the inner current loop should be greater than the cut-off frequency of the outer voltage loop. This would lessen the effect that the phase shifting of the current loop has on the voltage loop. In the low-frequency domain, the voltage loop plays an even more critical role, and the converter may be seen as the voltage source in this context. To ensure that the current control mode functions with a rapid dynamic reaction, the current loop is critical in the high-frequency area of the frequency spectrum. When the system runs in closed-loop control mode, the loop gain must fulfil the stability criteria by maintaining a phase-angle margin of at least 45 degrees and an amplitude margin of at least 6 DB. Therefore, the notions must be considered while selecting parameters in the circuit's component sections.

The PI stage 1 and PI stage 2 controllers are designed with Type II compensators widely used in power converters' control loops. Each type II compensator has two poles and one zero, and the zero is placed somewhere between the poles. These compensators are used to provide a phase boost to the control loop. Subsequently, these compensators reject low-frequency signals. The cutoff frequency of the compensation has been designed to block the second-order frequency of the ripple. In each PI stage, four passive circuit components are needed. The transfer function of the closed

compensator can be derived and given by the PI stage in equation (6).

$$G_v(s) = \frac{sC_2R_2+1}{R_1C_1s(sC_{12}R_2+1)} \quad (6)$$

where C_{12} is the parallel combination of C_1 and C_2 and given by equation (7),

$$C_{12} = \frac{C_1C_2}{C_1+C_2} \quad (7)$$

The transfer function of the closed compensator can be derived and given by for PI stage 2 in equation (8),

$$G_i(s) = \frac{sC_5R_5+1}{R_3C_4s(sC_{45}R_5+1)} \quad (8)$$

where C_{45} is the parallel combination of C_4 and C_5 in equation (9),

$$C_{4,5} = \frac{C_4C_5}{C_4+C_5} \quad (9)$$

When the output voltage frequency of the inverter is 50Hz, the input current of the Push-pull converter would contain the 100Hz low-frequency ripple component. From the above analysis, the error voltage signal also includes the 100Hz low-frequency ripple. For the design values of the PI stage 1 controller R1= 680kΩ, R2 = 1MΩ, C1= 22nF and C2=100nF and the transfer function of PI stage1 is given in equation (10)

$$G_v(s) = \frac{-66.8s-668.45}{s^2+55.45\,s} \quad (10)$$

PI stage 1 transfer function has one zero and two poles. The gain margin is infinite, with a gain cross-over frequency of 40.8 Hz and a phase margin of -50.1. The system is hence stable. The system is thus stable. The bode plot's reaction is depicted in Fig. 6.

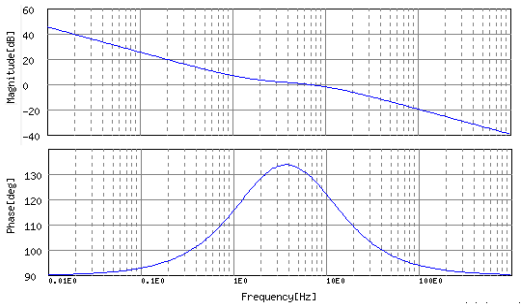

Fig. 6. The PI stage 1 controller bode plot response.

And similarly, for the design values of the PI stage 2 controller R1= 390kΩ, R2 = 390MΩ, C1= 5nF and C2=100nF. The transfer function is given in equation (11)

$$G_i(s) = \frac{-512.8s-13149.2}{s^2+538{,}46\,s} \quad (11)$$

It has two poles in addition to one zero. A phase margin of -27.1, a gain cross-over frequency of 73.2 Hz, and a gain margin of infinity are all specified values. Therefore, the system is in a stable state. The bode plot response is seen here in Fig.7.

Therefore, the Q value will likely decrease to strengthen the resonant controller's filtering capacity to various frequency ripples.

The DC-AC full bridge sinusoidal PWM controller will manage with a reduced DC-link voltage drop and maintenance of the AC output voltage as constant. While here, the input DC battery has a nonlinear discharge voltage characteristic.

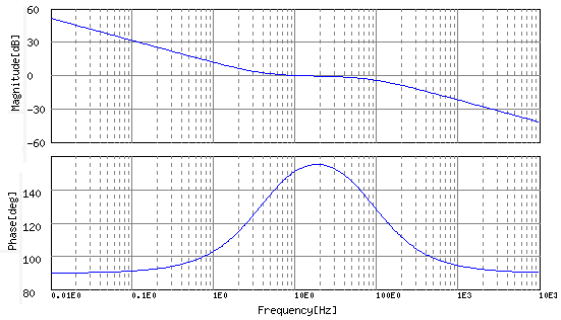

Fig. 7. The PI stage 2 controller bode plot response.

The schematic of a proposed dual closed-loop compensator is depicted in Fig. 8.

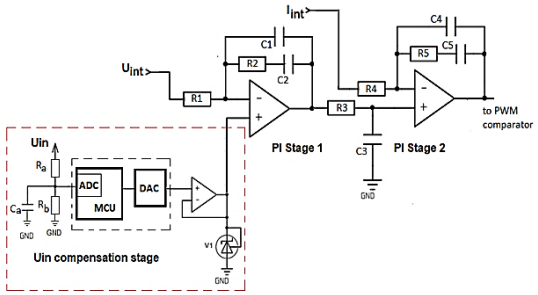

Fig. 8. The U_{in} compensation stage with Type II compensators.

As a result, a microcontroller-based signal processing unit has adapted to manage the battery voltage reference to the closed loop system. The battery voltage reference is given to the potential divider and then passed to the microcontroller that senses and defines the reference voltage to the PI stage 1 closed loop. This U_{in} compensation section sustains the closed loop. During the battery discharge condition, based on the consumption of AC output power, the intermediate DC link's voltage and current are regulated, and the ripple from the DC input current is managed and kept within an acceptable range. Based on the battery type and chemistry, the microcontroller's discharge characteristics are programmed as a loop-up table. Fig. 9 depicts the DC input voltage vs DC-link voltage closed-loop response.

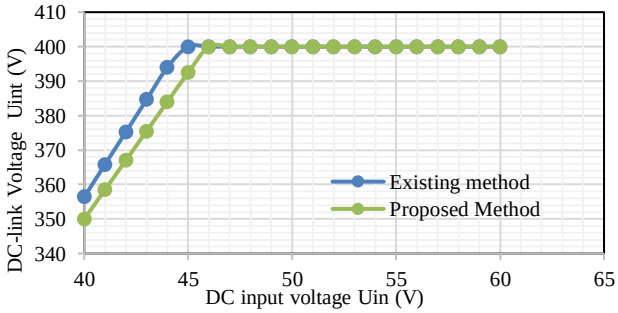

Fig. 9. Input vs. DC-link voltage closed-loop response.

The push-pull converter is designed to take a nominal input voltage of 48 V and convert it to 400 V. The converter reaches its maximum duty cycle at 45 V, and the DC voltage begins to reduce from 400 V. At a minimum input voltage of

42 V, the converter's U_{int} voltage is decreased to 350 V. The modulation index in the DC-AC inverter is adjusted to the PWM control of the DC-to-AC converter, which is intended to keep the output AC voltage at 230 V during low DC input operation.

4. CONVERTER DESIGN CONSIDERATION AND ANALYSIS

4.1 Transformer design

The push-pull transformer operated with a maximum duty cycle of 50%. A transformer's turns ratio is set to achieve maximum efficiency at the nominal operating voltage. Considering the minimum operating voltage of 42 V, the converter's switching frequency of 100 kHz, and the total power considered for this design, there was a total of 1 kW. To reduce leakage inductance, a secondary winding is placed close to the core without a bobbin in the first layer, over that primary winding as a bifilar winding, that aids in balancing the current in two primary windings and achieving good coupling. The triple-insulated wire was chosen to meet the clearance and creepage safety requirements. The transformer rating is designed based on the converter used in the circuit and the output power delivered. The design method is based on the K_g core geometry approach (Graovac et al., 2009). Here, the transformer power rating is directly related to the area of the product transformer. Various materials are analyzed based on the ferrite core material type results, and finally, N97 core material is selected for the transformer.

$$P_t = \frac{P_o}{\eta} + P_o \tag{12}$$

Equation (12) is used to calculate the total power of the transformer. In this design, transformer efficiency is considered to be 98%.

$$K_e = 0.145\, {K_f}^2 f^2 Bm^2 (10^{-4}) \tag{13}$$

Equation (13) is used for calculating the electrical condition of the transformer. In the equation, K_f is the waveform coefficient, and Bm is the maximum flux density.

$$K_g = \frac{P_t}{2K_e\alpha} = \frac{W_a A_c K_u}{mt} \tag{14}$$

The core geometry for the transformer can be calculated using equation (14). W_a represents the core winding area, Ac represents the core cross-sectional area, K_u represents the window utilization factor, and mt represents the mean length per turn. The design involved operating the inverter at 50 ˚C, the maximum operating temperature at full load. From this equation, the ETD54 core size matches the power of the 1 kW transformer design.

$$N_p = \frac{U_{in-min} D_{max} T}{\Delta B A_C} \tag{15}$$

The primary number of turns for the transformer is calculated using equation (15), where ΔBis the change in magnetic flux and A_c is the core area. From this equation, the required number of primary winding turns is 6. The transformer's turn ratio is 1:10.

4.2 Converter Output Inductor and Capacitor Design

The output filter inductor is calculated from the I_{int} ripple current. Here, the percentage of ripple is assumed to be 30%.

$$I_{int}{}^{pk} = I_{int} + \frac{\Delta I_r}{2} \tag{16}$$

$$U_t = \frac{Uin_{\mathrm{pk}}\, x\, N_S}{N_P} \tag{17}$$

$$energy = \frac{L_1\, Iint_{pk}^2}{2} \tag{18}$$

Equation (16) calculates the peak DC-link current passing through the inductorL_1 . Equation (17) defines to evaluate the maximum output voltage of the diode bridge. The energy stored in the inductor is given by equation (18). The design method is based on the K_g core geometry approach. The size of the core

$$L_1 = (U_t - U_{int}) x \frac{D_{min}}{2 x f_s x \Delta I_r} \tag{19}$$

We get this 1.5 m H inductor value from the above equation (19). Making the powder cores using the filter inductor can minimize the eddy current loss. The core size is determined by the peak current passing through the inductor. The core geometry for the transformer can be calculated using equation (20).

$$N = \sqrt{(L/A\_L)} \tag{20}$$

From the magnetic core datasheet, the core has been chosen. Equation (18) shows how to calculate the inductor number of turns from the core specification sheet. From this equation, the required number of inductor winding turns is 80. The C1 capacitor ripple voltage will be calculated using the following equation (21).

$$C1 = \Delta I_r\, x\, \frac{D_{min}}{2 x f_s x\, 8\, x \Delta U_{int}} \tag{21}$$

Increasing the value of the DC link intermediate capacitance, the ripple in the DC input current can be reduced. The above equation (21) can get this 720 µF inductor value.

4.3 Filter Inductor and Capacitor Design

The L_{in} and C_{in} DC inputs are built with a low pass filter that will be calculated using the given equation (22). The DC input filter needs were lowered using the active ripple reduction method, and the cutoff frequency for this design is considered less than 1 kHz.

$$\text{Cutoff frequency } \mathrm{f}_c = \frac{1}{2\sqrt{LC}} \tag{22}$$

Similarly, for the inverter AC output, L_{filter} and C_{filter} are designed as a low pass filter, and this will be calculated by the given equation (22). The output filter cutoff frequency is designed based on the switching frequency of the inverter, and for this design, the cutoff frequency is considered less than 2.5 kHz.

5. EXPERIMENTAL PROTOTYPE CONSTRUCTION AND TEST SETUP

The proposed method, a TSI using the push-pull converter implemented practically, and the performance of the proposed ripple reduction scheme has been analyzed with different types of loads. The converter load impact on the system's dynamic response is analyzed, and results are presented. In addition, transformer design, power loss and

thermal, efficiency of the inverter, and response are being investigated for the proposed system. The push-pull converter prototype experimental laboratory setup is shown in Fig. 10. The push-pull converter is operated using Q1 and Q2 MOSFET power devices. The nominal input voltage (U_{in}) is 48 V, indicating the battery's source. The DC input operating range of the inverter is from 42 to 60 V. For the inverter application, the nominal transformer design power rating is 1 kW.

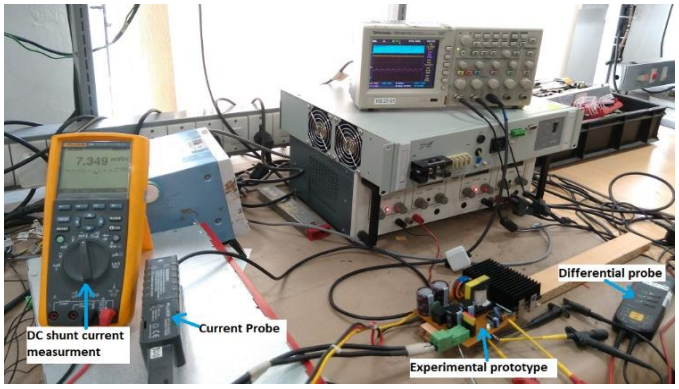

Fig. 10. Overall experimental setup.

The efficiency is assumed for this converter-designed calculation to be more significant than 95%. The switching frequency is 50 KHz. The initial DC-DC conversion stage transforms 48 to 400 V using a transformer constructed at a 1:10 ratio. At the source, the inductor (L_{in}) is 11 µF, the capacitor (C_{in}) is rated at 4400 µF, and the transformer secondary square pulses are rectified to DC using the D1-D4 diode full bridge. The capacitor (C_1) is rated at 720 µF/450V, and the inductor (L_1), rated at 1500 µH is used as a DC-link stage filter. The front-end push-pull converter PWM triggering pulses are generated using the UC2525 PWM controller with the LM2903 operational amplifier, and the dual closed-loop control schemes are implemented in the design. The converter design parameters are tabulated in Table 1.

Table 1. Push-pull DC-DC converter specification.

Parameter	Values
Switching frequency	50 kHz
operating range U_{in}	48V (42-60)
Nominal-output power	1kW
Nominal-output voltage U_{int}	400V
DC-DC transformer ratio	1:10
Inductor L_{in}	11 µF
Capacitor C_{in}	4400 µF
Capacitor C_1	720 µF
Inductor L_1	1.5 mH

The second stage is a full bridge DC-AC inverter. The DC-link voltage is 400 V supplied to the full bridge IGBT section. This is controlled by using the Atmel 328 microcontroller. It generates the level three sinusoidal PWM triggering signal to the IGBT T1, T2, T3, and T4 for producing the AC sine wave output. The inverter output voltage is 230 V load output at a frequency of 50 Hz. The polypropylene film type capacitor (C_{filter}) is rated at 4.7 µF/275 V, and the inductor (L_{filter}) of 900 µH is used at the output of the IGBT section, that converts the pulsated sinusoidal square waveform into AC. The circuit uses the LC differential filter to suppress the high-frequency signal. In Table 2, the specifications of the TSI topology are listed.

Table 2. Proposed inverter specification.

Design parameters	Values
U_{load} voltage	230 V
I_{load} current	3.5 A
Inverter output supply frequency	50 Hz
DC to AC conversion frequency	19.5 kHz
Output filter capacitance C_{filter}	4.7 µF /275 V
Output filter inductor L_{filter}	900 µH
Output Power rating (W)	0.8 kW

During the practical implementation, the proposed method is tested at 48 V and 42 V operating voltage ranges, and the load is about 800 W. The inverter steady state AC output waveforms and DC input voltage, and current waveforms are measured using DSO. Fig. 14 shows the DC source current ripple at 48 V nominal operating voltage response.

6. PERFORMANCE ANALYSIS OF PUSH-PULL CONVERTER:

6.1 Inverter Performance and Thermal Analysis

The final inverter output is connected to the resistive load and gives the inverter 800 W of absolute power. Table 3 shows the switching devices used in the DC-DC converter and DC-to-AC inverter.

Table 3. Power devices used in the prototype experimental inverter.

Part number	Parameter
MOSFET - Q1, Q2 IRFP4127PBF	U_{ds}=200 V, I_d=54 A at T_c=100˚C, $R_{ds}(on)$= 17 mΩ
Diode MUR880E - D1, D2, D3, D4	U_R= 800 V, I_{avg}= 8 A at T_J=150˚C, V_f = 1.5 V at T_J=150˚C
IGBT STGP19NC60KD - T1, T2, T3, T4	U_{ces}=600 V, I_c=20 A, T_c=100 ˚C,U_{ce} (sat) = 1.65 V, T_c=100 ˚C E_{on}=250 µJ, E_{off}= 445 µJ

During the practical implementation, the proposed method is tested at a 48V DC with a load of about 800 W giving the inverter an overall efficiency of 91.5%. The DC-DC converter, DC-AC inverter, transformer, and filter inductance power loss are evaluated. The DC-DC converter efficiency is 95.3%, and the DC-to-AC inverter efficiency is about 96%. The DC-DC converter and DC-to-AC converter power devices switching, and conduction loss are evaluated using theoretical equations. This switching power loss is estimated at 48V operation, and the overall inverter significant components power loss is plotted in Fig.11.

The transformer and filter inductance dc resistance is measured using an LCR meter and considered for the power loss calculation (Graovac et al., 2006; Salehahari et al., 2019; Assadi et al., 2019; Savitha and Kanakasabapathy, 2016). Table 4 shows the evaluation of the power loss of the inverter. The experimental prototype of the push-pull

converter section thermal camera view is portrayed in Fig. 12.

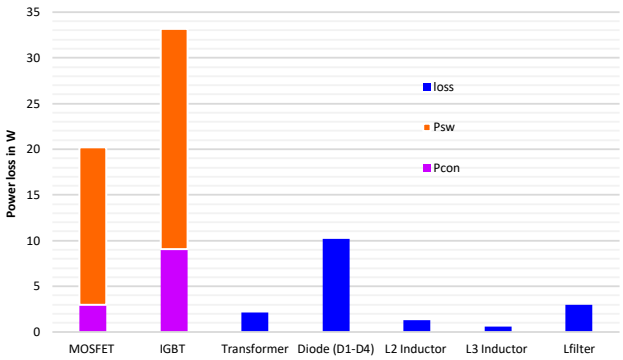

Fig. 11. Evaluation of energy loss of the proposed inverter.

Table 4. Proposed inverter Power loss evaluation.

Power Devices	Loss (W) at 48V
MOSFET P_{con}	3.0
MOSFET P_{sw}	17.2
IGBT P_{con}	9.1
IGBT P_{sw}	24.1
Transformer Loss	2.1
Diode Loss	10.2
L2 Inductor Loss	1.3
L3 Inductor Loss	0.6
Auxiliary power	10.1
Loss in inductor L_{filter}	3.0

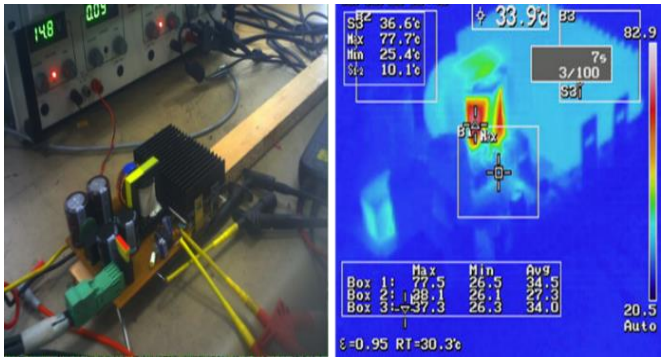

Fig. 12. Thermal view of the experimental setup.

An auxiliary fly-back converter is used for the inverter's internal circuit operation, and its power is also considered for the calculation. In the prototype picture, the DC-DC converter power devices are assembled with a heat sink assembly. The temperature measured using the thermal camera is about 37.3˚C, and the transformer measured a maximum temperature of about 77.7˚C.

6.2 Steady state response analysis

The closed-loop system performance was further investigated with different types of loads. The U_{load}, I_{load}, U_{in}, and I_{in} waveform static responses are captured in a DSO. With the AC output load, current phase angle shift lag or lead or peak influences the battery current ripple. The experimental prototype is tested with an RC load of 800 W/1 kVA, and 0.8 pf results are shown in Fig. 13.

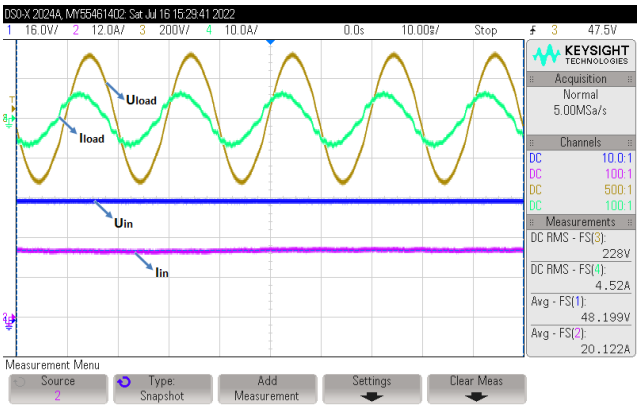

Fig. 13. Proposed method output loaded with RC load of 800W /1kVA load.

The AC output waveform shows that the I_{load} load current leads to the output voltage. In contrast, the I_{in} battery current has no significant ripple, ensuring the proposed method is stable with the RC load response. Most of the telecom inverters are critical load would be a computer power supply with a low power factor and high crest factor response. Considering this field's actual load condition, it is also tested with a non-linear load of 700 W/1 kV A, 2.5 CF and 0.7 PF with the help of chroma electronic load model 63803. and responses are shown in Fig. 14.

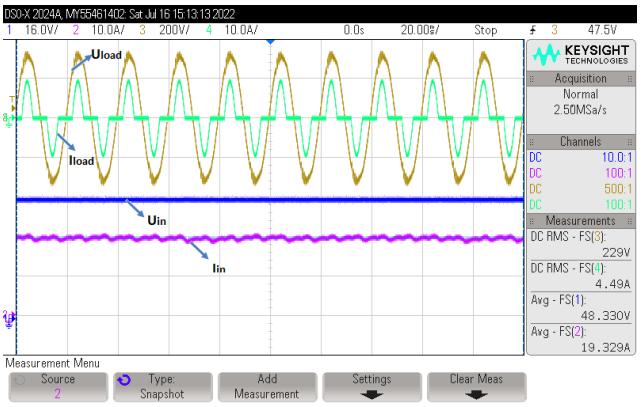

Fig. 14. Proposed method output with a non-linear load of 700 W/1 kV A, 2.5 CF and 0.7 PF tested with Chrome electronic load model 63803.

The AC output waveform shows that the I_{load} load current has a sudden 2.5 times peak. The ripple current is 0.45 A, and the average current is 19.3 A. The ripple is reduced by about 2.3%, In contrast, the I_{in} battery current has minimal ripple and within acceptable limits, ensuring the proposed method is stable with the non-linear load response. With the RC load and non-linear load, the load current characteristics change by phase and amplitude, and the system maintains a closed loop and controls the input current ripple. The proposed method works perfectly with different load types on the steady-state response.

6.3 Dynamic response analysis

The dynamic response has been verified in an experimental prototype setup. The U_{load}, I_{load}, U_{in}, and I_{in} waveform dynamic responses are captured in a DSO at 42 V. Fig. 15 shows a resistive load of 800 W,

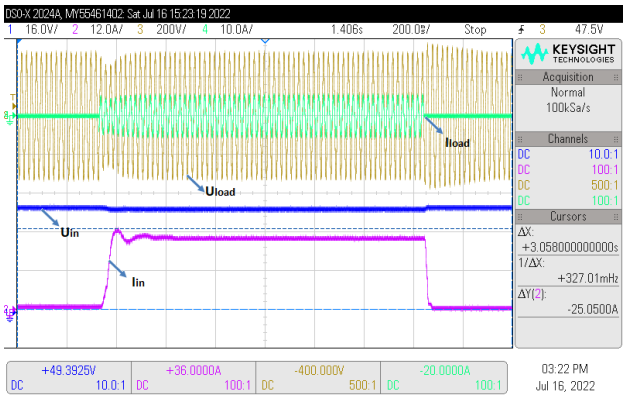

Fig. 15. Waveform dynamic response with Resistive load 800W.

In sudden load impact with 800 W resistive load, the I_{in} current is settled within 100ms and ripple in control. Similarly, Fig. 16 shows an RC load of 800 W/1 kVA and 0.8 pf results.

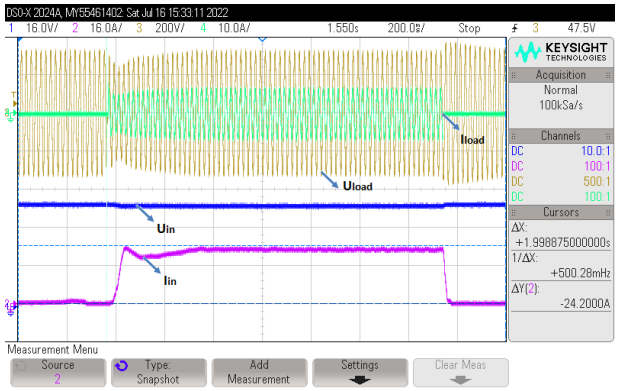

Fig. 16. Waveform dynamic response non-linear computer load simulated with Chrome an electronic load model 63803.

With the sudden load impact with 800 W/1 kVA RC load, the I_{in} current is settled within 100ms and ripple in control. In above dynamic response, the I_{in} well maintain by the proposed closed-loop system sustained within 100 ms of duration for the resistive and RC load and the battery input current is steady and ripple-free.

7. COMPARISON OF THE RIPPLE RESPONSE TO BOTH SCHEME SIMULATION AND EXPERIMENT RESULTS.

7.1 Analysis of existing scheme response

The existing and proposed method of closed loop system has been modeled in a PSIM simulation tool. The existing closed-loop scheme controls the ripple at the nominal operating voltage. When a battery runs out of power, its voltage drops while the PWM duty cycle of the push-pull converter goes up to its highest value. At this point, the PI stage 1 U_{int} voltage compensator becomes an open loop, the ripple reduction control system fails, and ripples appear in the inverter input current. Due to the open loop operation of the DC-DC converter system, the current ripple starts from 45 to 42 V. This study analyses the TSI inverter DC input current ripple with an 800 W resistive load at a minimum operating voltage of 42 V. The input DC source current response of the simulation result is plotted in Fig. 17.

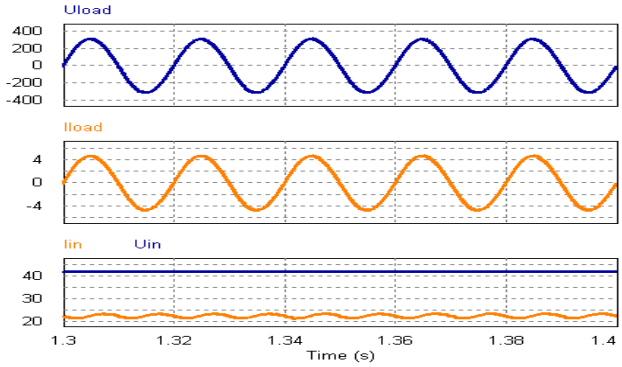

Fig. 17. Simulation results of existing closed loop system.

During minimum voltage operation at 42 V, it was observed that the existing control method produces current ripples. The ripple current I_{in} was found to be 2.24 A, with an average current of 22.35 A and a ripple percentage of 10%.

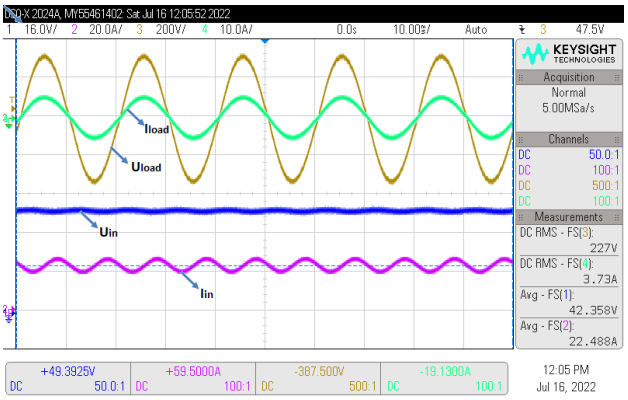

Fig. 18. Experimental results of a proposed dual closed loop with battery DC input reference.

The same test condition was verified in the experimental test setup, which also showed the presence of ripples in the input current waveform. At 42 V operation, the I_{in} current ripple was measured to be 2.3 A at the specified load. The average current was approximately 22.49 A, with a ripple percentage of 10.2%. Fig. 18 shows that the Experimental results of a proposed dual closed loop with battery DC input reference.

7.2 Analysis of Proposed Scheme Response

The existing closed loop has been adapted with a U_{in} compensation stage and minimum operating voltage simulation response captured. From Fig. 19, the simulation results show that the DC input current ripples disappear, and the proposed closed-loop system is employed. In an existing system, by introducing the DC input reference feedback, the ripple current of 0.45 A was reduced by about 2.2% and the average current of 20.5 A was maintained. The U_{int} voltage is regulated at minimum operating voltage, and the closed-loop system is stable.

In the same way, Fig. 20 shows the experimental analysis of the battery current ripple response at 42 V, and the ripple in the input current is 0.306 A at a load of 42 V. The average current is about 21.88 A, and the ripple percentage is 1.4%.

The proposed method was to reduce the I_{in} current ripple in minimum operating voltage of the inverter and furthermore, it

offers a ripple free operating the entire operating voltage of the inverter.

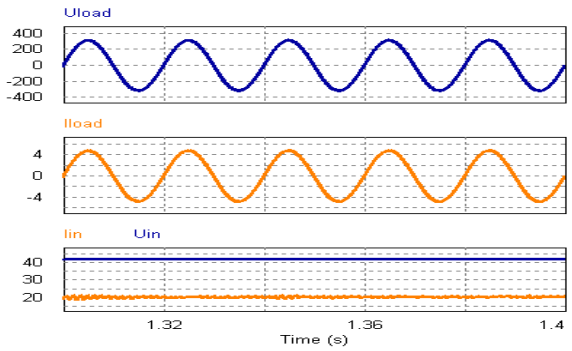

Fig. 19. Simulation results of the proposed closed-loop system.

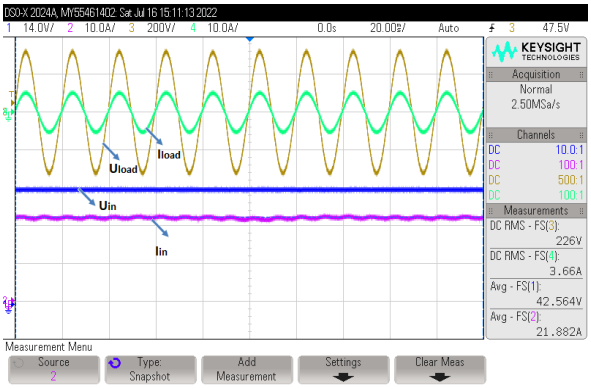

Fig. 20. Experimental results of proposed dual closed loop with battery DC input reference.

The proposed closed loop system is stable. Additionally, the telecom standard the psophometric was conducted at the DC input port, and it meets the telecommunication standard requirement. The percentage of input DC ripple comparison with simulation and experimental are shown in Fig. 21.

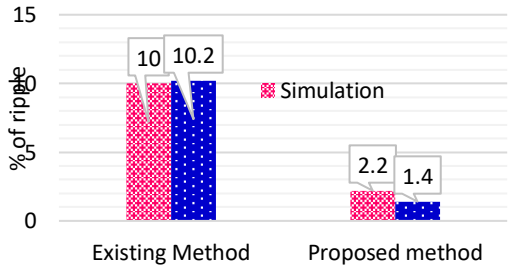

Fig. 21. Comparison of % of ripple with simulation and experimental response.

In summary, the U_{in} compensation has improved the closed-loop performance and controlled the ripple in the entire operating range of the inverter, and it meets the standard requirement.

7.3 Comparison analysis of ripple and efficiency

In the experimental setup, the inverter efficiency has been evaluated between existing and proposed methods at a worst-case operating voltage of 42 V dc input. The inverter load has been varied for efficiency evaluation from 0 to 800W. The existing process creates an open loop greater than a 500-watt load, and the input current ripple starts from this load. Due to the ripples, the power loss increases and the efficiency of the inverter decreases. At the same operating load condition, the proposed method has no ripple, and its efficiency is also good. The comparison of efficiency versus output power at a 42 V operating condition with both control methods is shown in Fig. 22.

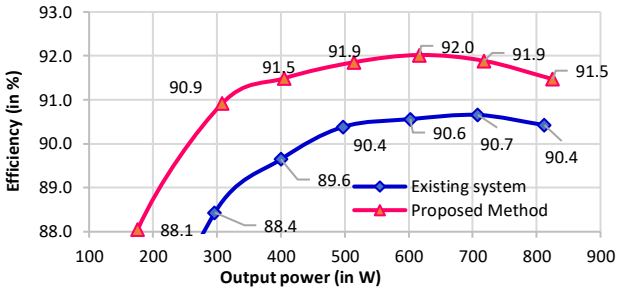

Fig. 22. Using both control methods, efficiency versus output power at 42 V operating conditions.

Similarly, the inverter input current percentage ripple has been evaluated over the entire operating range of the inverter with both control methods. In the existing control method, the input current ripple increases to less than 45 V onwards and it has reached to the maximum at 42 V ripple observed is 10.2%. The maximum ripple followed at the same operating voltage and load condition in the proposed control method is only 1.4%. The comparison of input current ripple versus various DC operating voltages with both control methods is shown in Fig. 23.

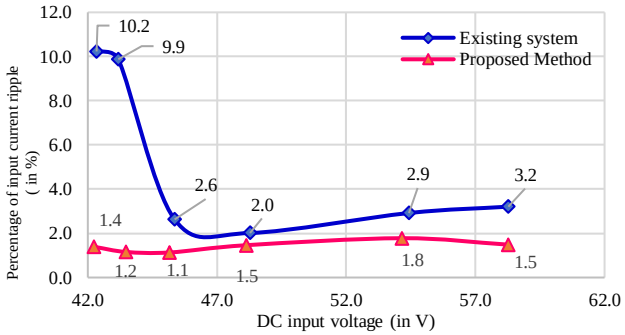

Fig. 23. Comparison of the ripple in the input current at different DC operating voltages with both control methods.

For recent technology batteries, the second-order ripple is a sensitive component that needs to be adequately controlled to avoid hazardous damage. The second-order ripple components have been optimized to introduce the battery voltage reference. However, since the study followed the simulation and experimental setup based on the 50 kHz converter switch frequency, this research can also be extended to the next level, optimizing other converter parameters.

8. CONCLUSION

This paper uses the existing dual closed-loop method to investigate the ripple in the DC input current in a TSI topology with a front-end push-pull converter. The existing scheme closed loop opens when the input DC voltage reduces, generating ripples at minimum voltage operation. This is investigated further, and a novel solution is proposed,

simulated, and validated. Compared to the existing method of ripple reduction at 42 V, a response of 10% is observed, and the same reaction with the proposed method is 2.2%. The practical consequence is that the input current ripple is about 1.4 % when operating at 42 V, and the simulation and experimental results match. The proposed method shows a significant improvement in the performance of ripple reduction compared to the existing method. Further, the ripple performance with various load types and the dynamic load response are validated on the experimental prototype. The proposed control system was stable with all responses. In addition, the proposed inverter efficiency and ripple response for entire operation characteristics are analyzed, and the results are good. Finally, the dual feedback with the proposed solution, the TSI system, provides reasonable control and maintains the DC input ripple. The ripple is reduced, and the obtained performance is good enough and compliant to meet the standard telecom requirements.

ACKNOWLEDGEMENT

This information is based on work supported by CET Power Solutions India Pvt. Ltd R&D department in India.

REFERENCES

ALE, A. A., and ABRISHAMIFAR, A. (2012). Low-Frequency Current Ripple Reduction in Two Stages Power Converter with a PI Controller and Nonlinear Gain.

Assadi, S. A., Matsumoto, H., Moshirvaziri, M., Nasr, M., Zaman, M. S., and Trescases, O. (2019). Active saturation mitigation in high-density dual-active-bridge DC–DC converter for on-board EV charger applications. *IEEE Transactions on Power Electronics*, *35*(4), 4376-4387.

Deng, H., Li, Q., Liu, Z., Li, L., and Chen, W. (2016). Low frequency current ripple mitigation of two stage three-phase PEMFC generation systems. *Journal of Power Electronics*, *16*(6), 2243-2257.

Dixit, S., and Rashmi, D. (2015). Half-bridge current-fed DC/DC converter for fuel/PV cell application. *International Journal of Emerging Technology in Computer Science & Electronics*, 14(2).

Graovac, D., Purschel, M., and Kiep, A. (2006). MOSFET power losses calculation using the data-sheet parameters. *Infineon application note*, *1*, 1-23.

Ivanovic, Z., and Knezic, M. (2022). Modeling Push–Pull Converter for Efficiency Improvement. *Electronics*, *11*(17), 2713.

Jain, S., and Agarwal, V. (2007). A single-stage grid connected inverter topology for solar PV systems with maximum power point tracking. *IEEE transactions on power electronics*, *22*(5), 1928-1940.

Jeyaraman, R., and Ravi, C. N. (2020, March). Low-frequency DC Input current ripple Reduction in a Two-stage Single-Phase Inverter using DC Input Voltage control. In *2020 6th International Conference on Advanced Computing and Communication Systems (ICACCS)* (pp. 342-347). IEEE.

Jung, H. J., and Kim, R. Y. (2014). A second-order harmonic current reduction with a fast dynamic response for a two-stage single-phase grid-connected inverter. *Journal of Electrical Engineering & Technology*, *9*(6), 1988-1994.

Lee, J. Y., Jeong, Y. S., and Han, B. M. (2011). A two-stage isolated/bidirectional DC/DC converter with current ripple reduction technique. *IEEE Transactions on Industrial Electronics*, *59*(1), 644-646.

Lu, N., Yang, S., and Tang, Y. (2017). Ripple current reduction for fuel-cell-powered single-phase uninterruptible power supplies. *IEEE Transactions on Industrial Electronics*, *64*(8), 6607-6617.

Musarrat, M. N., Islam, M. R., Muttaqi, K. M., and Sutanto, D. (2021). Shunt active DC filter to reduce the DC-link ripple current caused by power converters to improve the lifetime of aluminum electrolytic capacitors. *IEEE Transactions on Industry Applications*, *57*(4), 4306-4315.

O'Connor, J., Leonard, T., and Bohensky, G. Comparing Methods To Determine The Health Of Battery Systems. *BTECH, Inc., Rockaway*.2021

Ramakrishnan, J., and Ravi, C. N. (2022). Optimization of passive filter components through active filtering of current ripple reduction in an inverter. *International Journal of Power Electronics and Drive Systems (IJPEDS)*, *13*(1), 298-308.

Salehahari, S., Babaei, E., Hosseini, S. H., and Ajami, A. (2019). Transformer-based multilevel inverters: analysis, design and implementation. *IET Power Electronics*, *12*(1), 1-10.

Savitha, K. P., and Kanakasabapathy, P. (2016) Multi-port DC-DC converter for DC microgrid applications. In *2016 IEEE 6th International Conference on Power Systems (ICPS)* (pp. 1-6). IEEE.

Shi, Y., Liu, B., and Duan, S. (2015). Low-frequency input current ripple reduction based on load current feedforward in a two-stage single-phase inverter. *IEEE transactions on power electronics*, *31*(11), 7972-7985.

Shi, Y., Liu, B., and Duan, S. (2018). Modelling, control and performance analysis of a single-stage single-phase inverter with reduced low-frequency input current ripple. *IET Power Electronics*, *11*(6), 1074-1082.

Wei, Z., Deng, X., Gong, C., Chen, J., and Zhang, F. (2012, October). A novel technique of low frequency input current ripple reduction in two-stage dc-ac inverter. In *IECON 2012-38th Annual Conference on IEEE Industrial Electronics Society* (pp. 139-143). IEEE.

Xu, S., and Ji, Z. (2016). A Study of the SPWM High-Frequency Harmonic Circulating Currents in Modular Inverters. *Journal of Power Electronics*, *16*(6), 2119-2128.

Yang, P., Cao, J., Shang, Z., Cai, Y., and Xu, J. (2019). Double-line frequency ripple suppression of a quasi-single stage AC–DC converter. *IEEE Transactions on Circuits and Systems II: Express Briefs*, *67*(10), 2074-2078.

Zhang, L., Ruan, X., and Ren, X. (2017). Second-harmonic current reduction for two-stage inverter with boost-derived front-end converter: Control schemes and design considerations. *IEEE Transactions on Power Electronics*, *33*(7), 6361-6378.