Hardware In Loop Cosimulation of LMS Algorithm for Shunt Active Filter to Mitigate Harmonics and Reactive Power - Xilinx System Generator Approach

R. Sriranjani*, S. Jayalalitha**

School of Electrical and Electronics Engineering
SASTRA, Thanjavur, Tamilnadu, India
*(e-mail: *mathusri@eee.sastra.edu, **sj_instru@eie.sastra.edu)*

Abstract: The performance of the shunt active filter depends mainly on the reference current generator and pulse generator which switches the active devices. This maintains the supply current near to unity power factor and sinusoidal. Hence, the objective of the paper is to develop a control algorithm for shunt active filter using Xilinx system generator to achieve sinusoidal current waveform with unity power factor. Many research works discuss about adaptive filter using Least Mean Square algorithm with multiple parameters. However, the complexity of the algorithm increases with increase in parameters. So, LMS algorithm with minimum parameters is mandate. Therefore, the proposed algorithm with minimal parameters is developed in digital simulator and prototyping DSP/FPGA board. In this paper, an adaptive filter is developed in system generator tool box in MATLAB and Spartan 6 Field Programmable Gate Array board is used as Hardware In Loop Cosimulation system. The adaptive filter extract the fundamental real component of the load current and voltage control loop generates the reference current. The indirect current control technique is adopted and the gating pulses are generated by Hysteresis controller. The control algorithm results exhibit sinusoidal current waveform with near to unity power factor which proves the efficacy of the algorithm.

Keywords: Shunt Active Filter, Current control algorithm, Adaptive filter, Hardware In Loop Cosimulation, Xilinx system generator, Spartan FPGA.

1. INTRODUCTION

The effective performance of Shunt Active Filter (SAF) depends on the control algorithm developed for reference current generation (Vinod et al., 2017; Jeraldine et al., 2014; Zhong et al., 2005). One such control algorithm is an adaptive filter. The adaptive filter is a computational device that iteratively models the relationship between the input and output signals of a filter. The filter self-adjusts the coefficients according to an adaptive algorithm. There are different types of filter configurations such as system identification, noise cancellation, linear prediction and inverse systems. The adaptive algorithms update the weights using Least Mean Square Algorithm (LMS), Normalized LMS algorithm or Recursive Least Square (RLS) algorithm (Badoni et al., 2016). However, the existing algorithms result in high steady state error with slow response. Hence, to facilitate high adoption rate with minimum steady state error and further to have much resembled model of the system for fundamental current generator, noise cancellation system using LMS algorithm may be the suitable choice.

Further, the control algorithm can be a direct current control or indirect current control technique. The control algorithm developed in DSP / FPGA controller or programming based technology results in increased computational capacity and adaptability. Also, the execution time of the subsystem of the connected control methodology involves CPU utilization time and calculation idleness. Consequently, the performance of high frequency switching SAFs depends on multi-DSP controller (Zhuo et al., 2005; Hao et al., 2004; Lei et al., 2004). The entire calculation can be actualized on single-DSP utilizing a minimum number of data - based Low Pass Filter (LPF) and fast response is achieved which is presented (Chen et al., 2005). This implementation makes the entire system more complex and it may worsen the efficiency of the system and thus, mitigation of harmonics.

In such scenarios, Field Programmable Gate Array (FPGA) - based controller with parallel processing might be used. In this way, there is an impact on the implementation of various control strategies because of its simultaneous task. Moreover, FPGA empowers simple and quick response and fast prototyping through Hardware Description Language (HDL) (Rodriguez et al., 2005). These great attributes make FPGA as a powerful controller for fast calculations involved in discrete system (Chan et al., 2004; Castro et al., 2003; Juang et al., 2006; Parma et al., 2007; Chan et al., 2007). It additionally provides continuous calculations for modern control frameworks (Dubey et al., 2007; Du et al., 2007; Monmasson et al., 2007). Already, FPGA controller used in pulse generation for power electronic devices (Omar et al., 2005) and solid state control AC motor (Naouar et al., 2007; Cirstea et al., 2007). The FPGA gives adaptability and powerful calculation required to develop algorithms for fast acting SAF (Zhong et al., 2005). Literatures reveal the fact that either dspace or HDL is used to accomplish discrete

control algorithms. Nonetheless, Hardware In Loop Cosimulation is not attempted for control algorithm of SAF.

A new approach to design the SAF controller is the use of "Xilinx blockset" (XB) simulator operating under Matlab/Simulink environment to produce a VHDL code for FPGA (Jintakosonwit et al., 2002; Muralikrishna et al., 2014). The control algorithms are developed in the discrete-time mode with a clock frequency of 20MHz. In this case, the FPGA prototype board is connected to a desktop Personal Computer System via a Joint Test Action Group (JTAG) interface. A model has been created for the simulation and generation of VHDL code for the execution of the control algorithm in a FPGA board.

Hence, from the available pool of weight updating algorithms, LMS algorithm with minimum parameters is proposed. As the algorithm involves less number of parameters, it would result in reduced computational complexity. Further, MATLAB – Xilinx based Hardware In Loop Cosimulation is implemented. In this, the supply voltage, load current and supply current are measured by the transducers and are converted to digital values. The control algorithms are implemented in MATLAB – Xilinx and it generates switching pulses for the power devices of the SAF. The system configuration for the proposed technique is elaborated in the succeeding section.

2. SYSTEM CONFIGURATION

Fig. 1 shows the common structure of 3 – phase shunt active filter. The ideal characteristics of SAF make the system user friendly. Irrespective of the load, the SAF performance should be better. To operate the SAF in dynamic load condition, it is designed to meet maximum load. In addition, the performance of SAF depends on the gate pulse of the active devices. The pulses are generated by the hysteresis controller which is operated in indirect current control technique. The reference current is compared with the actual supply current by the hysteresis controller. The reference current generator extracts the fundamental real component from the load current. The fundamental current along with the voltage control loop PI controller generates the reference current in order to balance the supply active power and load active power. Voltage control loop is active during transient condition. The circuit diagram is given in Annexure – I. The SAF comprises inductor, dc link capacitor and active power devices. Optimal design of the following system parameters can enhance the performance of the system considerably (Khadem et al., 2014),

- Filter Inductor (L_f)
- DC bus capacitor (C_{dc})
- Reference dc bus voltage($V_{dc,ref}$)
- Switching frequency (f_{sw})

Further, the values of passive components of filter are arrived based on the iterative procedure (Sriranjani et al., 2017) and the specifications are given in Annexure – II. Using the system design, the fundamental current extraction is carried out which is elucidated in the subsequent section.

3. FUNDAMENTAL CURRENT EXTRACTION

The load voltage and load current is given by

$$v_{rs}(t) = V_{mr} \sin \omega t \tag{1}$$

$$v_{ys}(t) = V_{my} \sin(\omega t - 120°) \tag{2}$$

$$V_{bs} = V_{mb} \sin(\omega t - 240°) \tag{3}$$

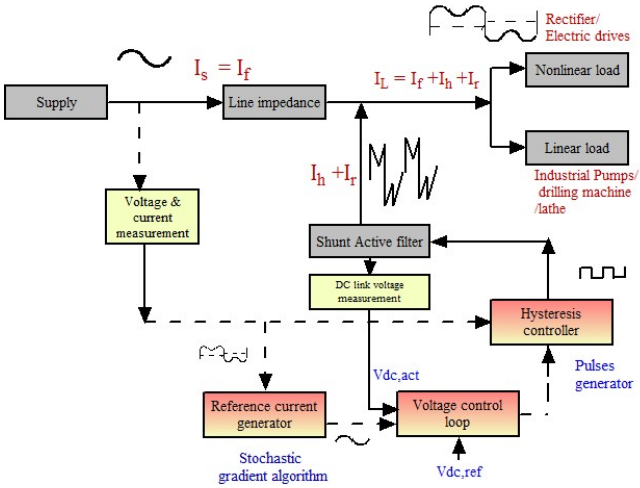


Fig. 1. System configuration.

$$i_{Lr}(t) = \sum_{h=1}^{\infty} I_{mrh} \sin(h\omega t - \varphi_{rh}) \tag{4}$$

$$i_{Ly}(t) = \sum_{h=1}^{\infty} I_{myh} \sin(h\omega t - 120° - \varphi_{yh}) \tag{5}$$

$$i_{Lb}(t) = \sum_{h=1}^{\infty} I_{mbh} \sin(h\omega t - 240° - \varphi_{bh}) \tag{6}$$

The general derivation of the adaptive filter is given below:

The adaptive filter is used as the fundamental real component extractor where the objective function is given by,

$$x(i) = \frac{1}{m} \sum_{j=1}^{m} x_j(i) \tag{7}$$

The weight is updated by LMS algorithm which is illustrated below:

$$we_{j+1} = we_j - \frac{\eta}{m} \sum_{j=1}^{m} x_j(i) \tag{8}$$

$$x(i) = \frac{1}{m} \sum_{j=1}^{m} x_j(i) = \frac{1}{m} \sum_{j=1}^{m} (d_j - y_j) \tag{9}$$

$$y_j = w_j v_j \tag{10}$$

where 'd' is the primary signal, 'y' is the output signal, 'w' is the weight, 'v' is the input variable, 'η' is the learning rate. From the LMS algorithm, the procedure for extracting fundamental real component from load current are derived and demonstrated below.

The three phase load current consists of active, reactive and harmonic current. Using LMS algorithm, the active current is extracted from the load current with reference to the input voltage and the voltage is assumed as sinusoidal voltage. The output signal is the fundamental real component of load current, primary signal is the load current and input variable is the supply voltage.

The load current is decomposed as

$$i_{Lr}(t) = I_{mr}\cos\varphi_{r1}\sin\omega t + I_{mr}\sin\varphi_{r1}\sin\omega t + \sum_{h=5,7,11,13}^{\infty} I_{mrh}\sin(h\omega t - \varphi_{rh}) \quad (11)$$

$$i_{fr}(t) = I_{mr}\cos\varphi_{r1}\sin\omega t \quad (12)$$

The input mains should supply the above fundamental current as the SAF injects the current $i_{safr}(t)$,

$$i_{safr}(t) = I_{mr}\sin\varphi_{r1}\sin\omega t + \sum_{h=5,7,11,13}^{\infty} I_{mrh}\sin(h\omega t - \varphi_{rh}) \quad (13)$$

The error signal $x(i) = i_{safr}(t)$, from equation (13) the error signal is written as,

$$x(i) = i_{safr}(t) = i_{Lr}(t) - i_{fr}(t) \quad (14)$$

The weight is updated by

$$we_{l+1} = we_l - \frac{\eta}{m}\sum_{j=1}^{m}\left(i_{Lrj}(t) - i_{frj}(t)\right) \quad (15)$$

$$i_{fr}(t) = \frac{v_{sr}(t)}{we_l} \quad (16)$$

The fundamental real component is extracted from the load current using LMS algorithm. The extracted reference current is given by,

$$i_{fra}(t) = I_{ma}\sin\omega t \quad (17)$$

For balancing the power between load and supply, the dc link voltage is controlled by PI controller and the reference signal is generated by adjusting the fundamental real component of load current with dc voltage controller gain.

The reference signal for R phase is given by,

$$I_{refa}(t) = i_{fra}(t)(K+1) \quad (18)$$

$$K = (v_{dc,ref} - v_{dc,act})K_p + (v_{dc,ref} - v_{dc,act})\frac{K_i}{s} \quad (19)$$

The reference current is sinusoidal in nature and it is compared with the actual supply current by hysteresis controller which generates gating pulses for Power MOSFET of SAF.

4. SIMULATION OF SHUNT ACTIVE FILTER

Simulation of SAF is carried out and the specification of software tools required for discrete controller is as follows:

- MATLAB - 7.10.0.499
- Simulink – 7.5
- Xilinx ISE design suite- 12.2

4.1 Simulation model

The simulation model of the system configuration is shown in fig. 2. The adaptive filter is designed using MATLAB simulink blocks and the power circuit is designed using power system block sets. The overall system configuration is given in Annexure – I. The learning rate considered for the adaptive filter is $5x10^{-4}$ for minimum value of THD which is shown in Table – 1. The adaptive filter using LMS algorithm generates the balanced three phase reference current which is sinusoidal in nature.

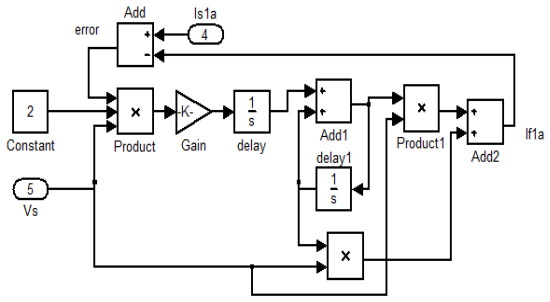


Fig. 2. Block diagram LMS algorithm.

Table 1. Learning Rate.

η	% THD
$1x10^{-4}$	5.3
$5\ x10^{-4}$	4.7
$1\ x10^{-3}$	5.117
$5\ x10^{-3}$	5.33

The control algorithm is tested for rectifier, induction motor and parallel operation of rectifier and induction motor load. Fig. 3 shows the voltage and current waveform of rectifier load, filter and supply. The supply current waveform is sinusoidal and in phase with the supply voltage. The FFT spectrum of load current and supply current shown in fig. 4 proves that the LMS based SAF mitigate harmonics from supply mains.

The three phase three wire supply is connected to the three phase induction motor. The supply current is sinusoidal in nature but it lags the supply voltage. The power factor of the supply current before compensation is 0.719. Fig. 5 shows that after compensation, the supply current is in phase with the supply voltage. Thus, the LMS based SAF current injects the fundamental reactive current to the supply mains. The FFT spectrum shows that reduction of supply current after compensation is illustrated in Fig. 6.

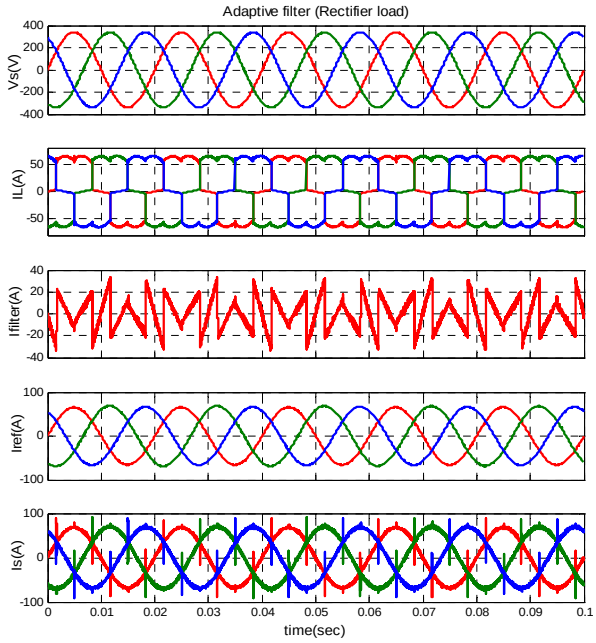


Fig. 3. Simulation results of voltage and current waveform of Load 1.

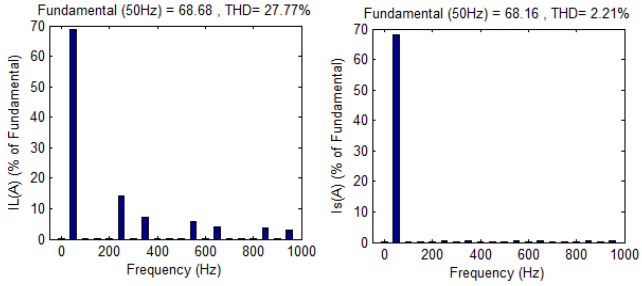


Fig. 4 . FFT Spectrum of load current and supply current of Load 1.

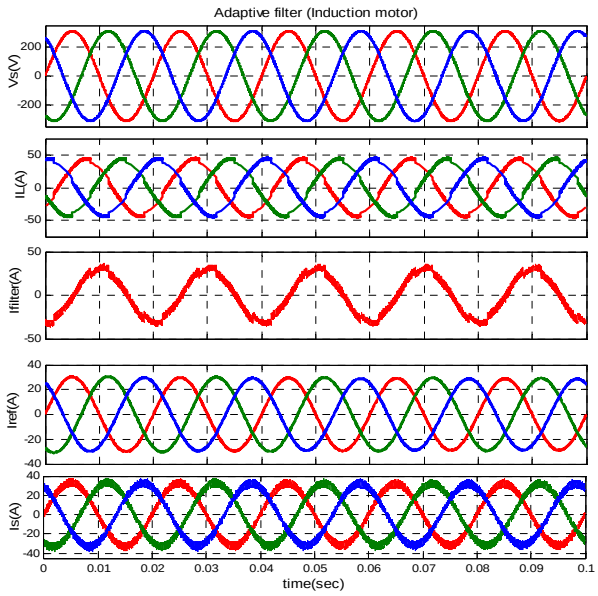


Fig. 5. Simulation results of voltage and current waveform of Load 2.

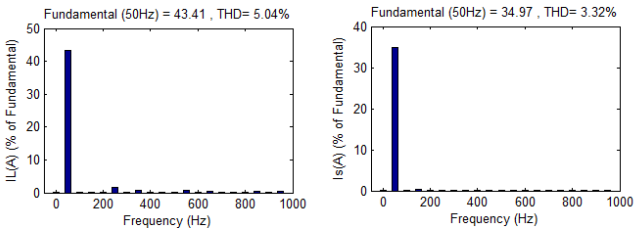


Fig. 6 . FFT Spectrum of load current and supply current of Load 2.

The control algorithm is tested in linear and non linear load conditions. The rectifier and induction motor is connected to the supply mains. The rectifier draws non sinusoidal current and induction motor draws active and reactive current. Fig. 7 shows that the filter injects harmonic current and fundamental reactive current. Thus, the supply is free from harmonics and reactive current. The FFT shows that the supply current draws only fundamental active component of the load current demonstrated in Fig. 8. Consequently, the LMS based algorithm is suitable for three phase three wire linear and nonlinear load. Table – 2 shows individual harmonics and total harmonic distortion of load 1 to load 3 (L1 to L3) respectively. Table – 3 shows the before and after compensation of supply side power factor and THD. For linear and nonlinear load, the supply power factor is near to unity and the THD is below 5% .

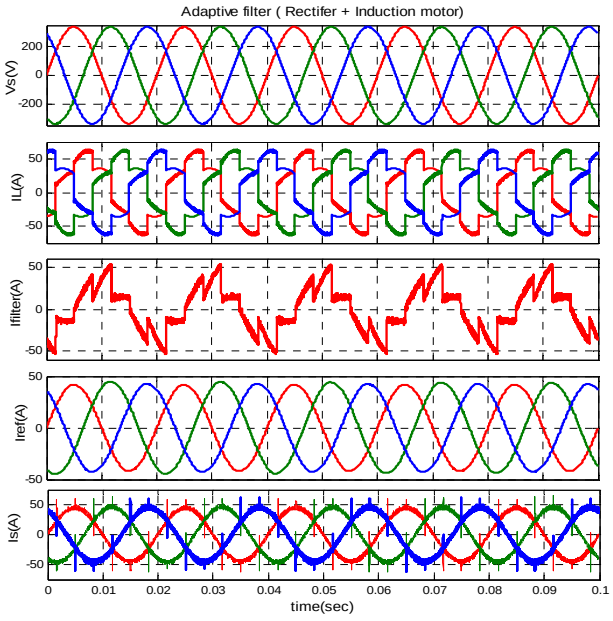


Fig. 7. Simulation results of voltage and current waveform of Load 3.

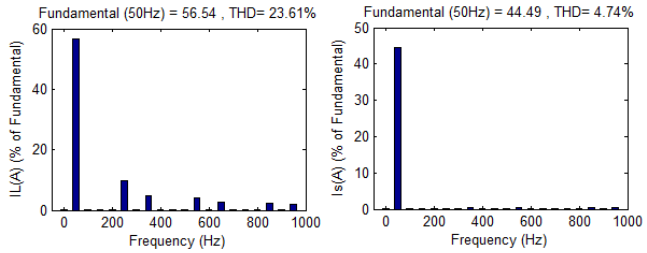


Fig. 8. FFT Spectrum of load current and supply current of Load 3.

Table 2. Harmonic analysis.

	Maximum Load current						
	5^{th}	7^{th}	11^{th}	13^{th}	17^{th}	19^{th}	THD %
L1	12.0	6.04	4.80	3.45	3.00	2.98	27.48
L 2	1.59	0.79	0.64	0.45	0.4	0.31	5.07
L 3	8	6.2	5.4	4.3	3.39	2.9	23.61

Table 3. Parameters of supply current.

	Supply					
	Before compensation			After compensation		
	Is (A)	pf	THD %	Is (A)	pf	THD (%)
Load1	50.34	0.944	27.48	48.65	1	2.21
Load2	30.69	0.719	5.07	24.7	0.999	3.32
Load3	41.09	0.751	23.61	31.49	0.996	4.74

5. DEVELOPING CONTROL ALGORITHM IN MATLAB XILINX

The development of control algorithm involves the following steps and is elucidated in the sub – section:

(i) Basic setting of the system generator
(ii) Building the blockset of control algorithm

5.1 Basic setting of the system generator

System generator specifications are depicted in Table – 4. The clock frequency of FPGA is 100MHz whereas developed system frequency is 20MHz. The clock input is applied at pin F13 of FPGA. For Analog to Digital conversion, a translator is required to convert 3.3 V to 5V and vice versa using SN74LVCC3245A and it functions as Bidirectional Voltage Translator. ON port A, converts 2.3V to 3.6V and ON port B converts 3V to 5.5V. The control inputs VIH/VIL levels should be an accessible reference to VCCA Voltage. The SN74LVCC3245A is intended for non concurrent correspondence between data buses and the device transmits information from bus 'A' to bus 'B' or from bus 'B' to bus 'A', contingent upon the logic level at the DIRection control (DIR) input. The Output Enable (OE) pin can be utilized to debilitate the device so that the bus is adequately segregated.

Table 4. System generator specifications.

System generator	Specifications
Compilation	Bitstream
Part	Spartan – 3A DSP XC3SD1800A-FG676-4
Target directory	./netlist
Synthesis tool	XST
Hardware description language	VHDL
FPGA clock period(ns)	50
Clock pin location	F13
Multi-rate implementation	Clock enables
Simulink system period	1

5.2 Blockset of control algorithm

5.2.1 Zero crossing detector

A reference point is required for zero crossing detection of the input signal and is determined by the supply voltage waveform. Analog circuits are designed to find the zero crossing of the R phase supply voltage. The square wave input is applied at pin 'AC3' and the 'Gateway In' pin is connected to the three phase zero crossing detector input. For unbalanced supply voltage, the three analog circuits are designed for three phase supply separately. The block diagram for the zero crossing detector is given in Fig. 9.

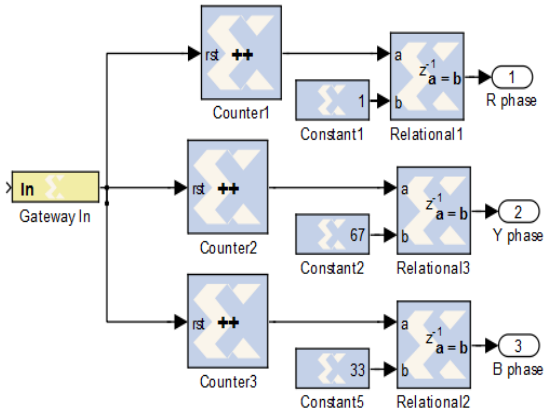


Fig. 9. Analog to digital conversion.

The analog signal is converted to digital by AD 7266 IC. The black box in Xilinx block- set used to configure the coding is illustrated in fig 10.

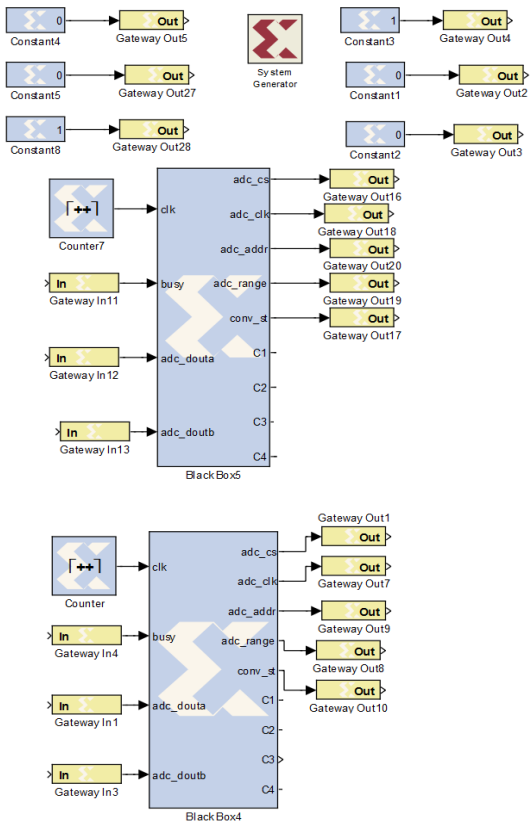


Fig. 10. Block set of Analog to Digital Conversion

The analog signal of three phase load current, supply current and DC bus voltage from the power circuit is converted to digital value. The 'Gateway Out' and 'Gateway In' represents the output and input of IOB pad pin selection of FPGA. The first set of C1 - C4 represents the digital value of three phase load current and B phase supply current. The second set of C1, C2 and C3 represent digital value of R and Y phase supply current and actual dc bus voltage. The high and low pulse is given to 'Gateway Out' according to pin selection. The reference voltage is set by the switch of the Spartan FPGA development board.

5.2.2 Discrete Adaptive filter using LMS algorithm

The discrete adaptive controller for a 3φ 3 – wire SAF using MATLAB - Xilinx System Generator is illustrated in Fig. 11. The integration is performed by the Down sample of Xilinx blockset and the learning rate of the adaptive controller is fixed. The 'addsub' and 'mult' block is used to achieve the fundamental current signal.

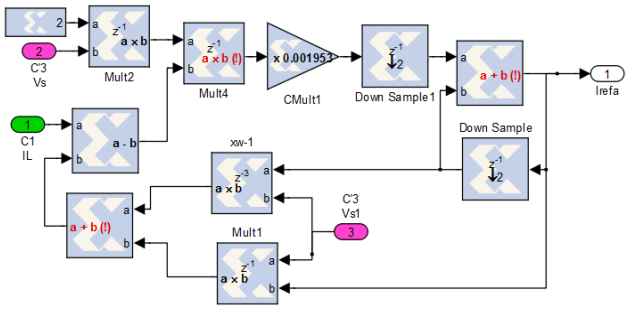


Fig. 11. Block set of Discrete Adaptive Filter using LMS algorithm.

5.5.3 Discrete voltage control loop

The coding for voltage control loop using a PI controller is developed in .m file and configured to FPGA through the black box. The reference current magnitude is generated from I_{refa} and gain of DC bus voltage controller is shown in fig. 12.

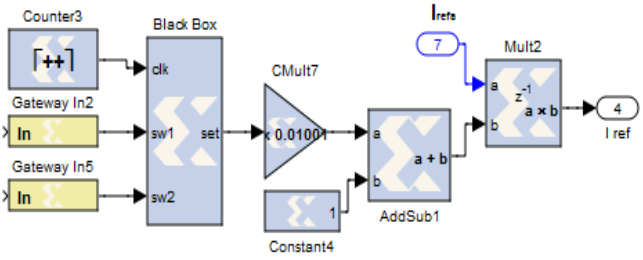


Fig. 12. Block set of voltage controller.

5.2.4 Discrete Hysteresis Current Control

The reference current is obtained by the trigonometric block of ROM1 and the I_{refa} generator block. The discrete current controller is implemented by arithmetic, logical and relational operator block illustrated in Fig. 13. The controller generates six pulses and it is given to the driver of Power MOSFET through FPGA PWM pin. The implemented FPGA based hysteresis current controller improves the system's immunity to noise by decreasing the hardware.

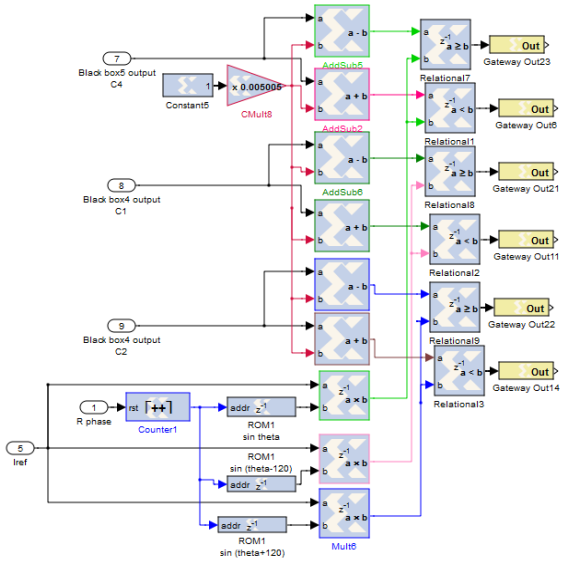


Fig. 13. Block set of Discrete Hysteresis Controller

5.2.5 Bit file generation for FPGA and communicated via JTAG Emulator

The developed algorithm in MATLAB Simulink environment generates "BIT File" (Machine language) using system generator. Xilinx ISE design suite 12.2 is interfaced to the FPGA through JTAG to download the bit file.

The system generator in Xilinx blockset generates the bit file and Impact Chain is initialized through Xilinx ISE design suite. Using boundary scan, the program is executed. When the JTAG is properly connected between the PC and SPARTAN 3A kit, the program is succeeded and loaded in FPGA. Once the program is loaded, a hardware circuit is interfaced with the FPGA processor through the 34 pin connector.

6. EXPERIMENTAL VALIDATION OF SHUNT ACTIVE FILTER

The theoretical and simulated results are validated by the hardware implementation of the system configuration. The control algorithms are developed in MATLAB Xilinx and it is interfaced via Xilinx ISE design suite to FPGA. The digital controller is preferred because of low power consumption and flexibility in parameter variation. The Spartan 3A FPGA kit guaranteed that the hardware design is reconfigurable, implies low cost development (reprogramming potential) and operate data more rapidly than a general purpose DSP. The input signals are in digital form, represented with an exact fixed-point format.

The computations of the algorithm involve saturation arithmetic for overflow handling and rounding for error quantization. The chip opted for developing the control algorithm is Xilinx XC3SD1800A-FG676-4 Spartan 3A FPGA, provided by XILINX Company. FPGA includes copious hardware resources and high frequency clock source. The digital controller has the sampling time of 50 µs while global clock period is 10ns. Xilinx system generator MATLAB tool blockset is used to generate bit file for FPGA.

The total complete streams, including examination, synthesis, mapping and routing are set up by Xilinx ISE design suite.

Fig. 14 shows the experimental setup of the system configuration. A 0.7kW, 10A six-pulse rectifier load is designed as a harmonic generator and the linear load of the induction motor of 0.5Hp is taken for this study. The 3φ line voltage is 120V and the reference dc bus voltage is 300V. The hardware circuit consists of a 3φ power supply, line impedance, 3φ diode bridge rectifier with RC load, Induction motor and SAF. The specifications of the hardware design are shown in Table 5.

Table 5. Hardware design specifications.

Devices	Specifications
3 – phase variac	415/(0-470) V, 15A
Current sensor(Hall effect transducer)	LTS 25 - NP
Source impedance per phase	120 µH,10A
Filter inductance per phase	1.5mH, 10A
Filter capacitance	1300µF, 900V
3-phase Intelligent Power Module	PM 25 RSB 120
Bipolar ADC	10V, 1MHz

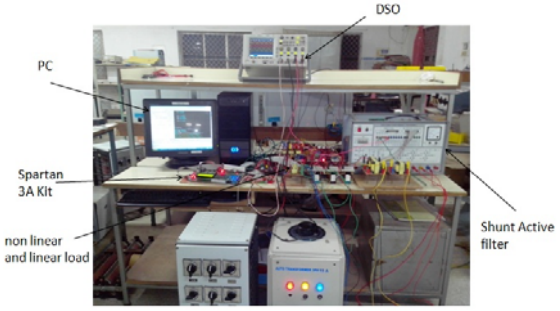


Fig. 14. Hardware setup of the overall system.

The filter comprises of the Intelligent Power module (Inverter), three numbers of coupling inductor and one number of dc link Capacitor. Six current transducers are used to measure the three phase load current and supply current and a voltage sensor measures the actual DC bus voltage of the SAF. There are three zero crossing detectors to obtain the zero crossing instant of the supply voltage. Precision Power Analyzer WT3000 is used to measure the THD of the current waveform at the source supply unit.

7. RESULTS AND DISCUSSION

The adaptive filter using LMS Algorithm generates the fundamental real component of the load current shown in Fig. 15. The fundamental current generated by the above algorithm is sinusoidal in nature and without phase shift which is observed in digital storage oscilloscope. The difference of reference current waveform and load current waveform gives the filter current waveform which is verified through the simulated results. Thus, the LMS based SAF injects harmonic current and the supply current is sinusoidal in nature. Further, it is in phase with the supply voltage demonstrated in Fig. 16.

Fig. 17 shows the experimental results of linear load. Before compensation the supply current lags the supply voltage and after compensation the supply current is in phase with the supply voltage. This clearly depicts the authenticity of simulated results. When both loads are connected to the supply mains and after switching on the SAF, the distorted supply current becomes sinusoidal and in phase with the supply voltage which is shown in Fig. 18. As the transient behaviour of the algorithm proves to be better, it is suitable for dynamic load variation condition shown in Fig. 19.

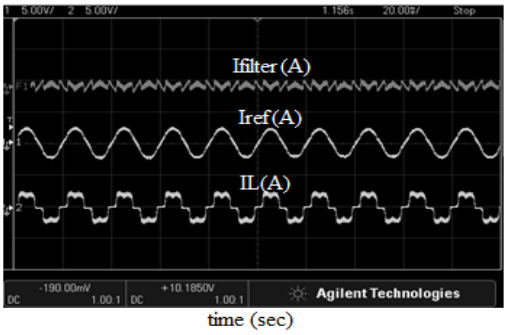


Fig. 15. Transient analysis of Reference current generated.

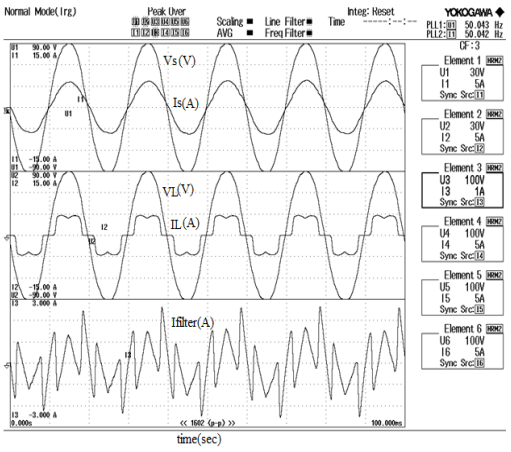


Fig. 16. Supply current, load current and filter current of Rectifier Load.

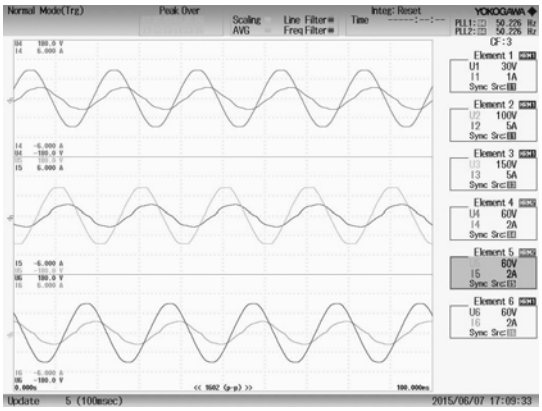


Fig. 17. Experimental results of three phase voltage and supply current waveform of Induction motor load(before compensation).

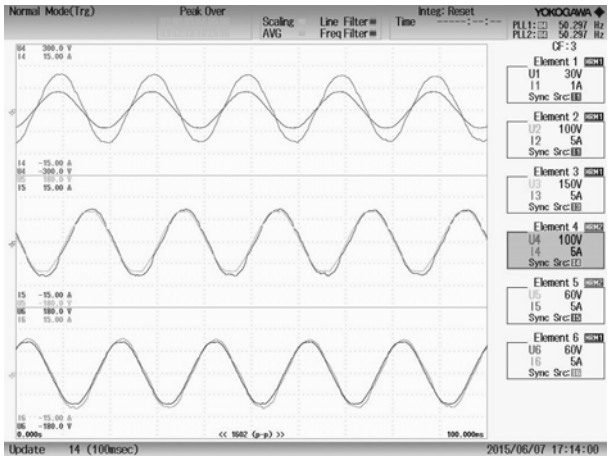


Fig. 18. Experimental results of three phase voltage and supply current waveform of Induction motor load(after compensation)

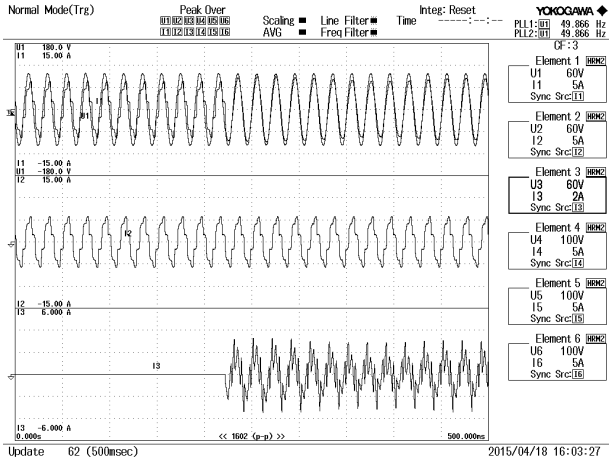


Fig. 19. Experimental results of voltage and current waveform of Rectifier and Induction motor load

To conclude, the control algorithm for SAF is proposed and validated through simulation and hardware. The results exhibits better transient response and improved power factor.

8. CONCLUSION

The shunt active filter acts as a harmonic mitigation device. To improve the performance of SAF, optimal control strategy for reference current generation is desired. In addition, the reference current influences the sinusoidal nature and power factor. Furthermore, the control algorithm ought to be validated through hardware. To achieve this, Least Mean Square based adaptive filter with minimal parameters is proposed. The proposal is simulated in MATLAB-Xilinx and implemented in hardware through Spartan FPGA development board. The control algorithm is developed in discrete time mode using Xilinx blockset and communicated to FPGA through Xilinx ISE Design suite and interfaced via JTAG. By interfacing the Simulink® model with Xilinx® ISE programming, it is conceivable to produce and synthesize a VHDL code effectively for FPGA usage. The hardware results exhibit that the LMS based SAF is viable in compensating current harmonics that encourages and enhances the power quality of the supply mains connected with the different types of load. The SAF is effectively compensating the current harmonics and makes the source current as sinusoidal for linear/nonlinear load and combination of a linear and nonlinear load. The FFT investigation of various load condition utilizing LMS confirms that the SAF decreases the THD of the source current below 5% in compliance with IEEE 519-2014 and IEC 61000-3 benchmarks of harmonics.

REFERENCES

Bo Sun, Ning-Yi Dai, U-Fat Chio, Man-Chung Wong, Chi-Kong Wong, Sai-Weng Sin, Seng-Pan U, Martins, R.P., “FPGA-based decoupled double synchronous reference frame PLL for active power filters”, IEEE Conference on Industrial Electronics and Applications (ICIEA), pp. 2145- 2150, 2011

Castro, A. D., Zumel, P., Garcia, O., Riesgo, T., & Uceda, J. (2003). Concurrent and simple digital controller of an AC/DC converter with power factor correction based on an FPGA. *IEEE Transactions on Power Electronics, 18*(1), 334-343. doi:10.1109/tpel.2002.807106

Chan, Y. F., Moallem, M., & Wang, W. (2007). Design and Implementation of Modular FPGA-Based PID Controllers. *IEEE Transactions on Industrial Electronics, 54*(4), 1898-1906. doi:10.1109/tie.2007.898283

Chan, Y., Moallem, M., & Wang, W. (2004). Efficient implementation of PID control algorithm using FPGA technology. 2004 *43rd IEEE Conference on Decision and Control (CDC)* (IEEE Cat. No.04CH37601). doi:10.1109/cdc.2004.1429572

Chen, Z., & Xu, D. (n.d.). Delayless harmonic detection based on DSP with high-accuracy for active power filter. *Twentieth Annual IEEE Applied Power Electronics Conference and Exposition*, 2005. APEC 2005. doi:10.1109/apec.2005.1453296

Cirstea, M., & Dinu, A. (2007). A VHDL Holistic Modeling Approach and FPGA Implementation of a Digital Sensorless Induction Motor Control Scheme. *IEEE Transactions on Industrial Electronics, 54*(4), 1853-1864. doi:10.1109/tie.2007.898286

Du, H., Qi, H., & Wang, X. (2007). Comparative Study of VLSI Solutions to Independent Component Analysis. *IEEE Transactions on Industrial Electronics*, 54(1), 548-558. doi:10.1109/tie.2006.885491

Dubey, R., Agarwal, P., & Vasantha, M. K. (2007). Programmable Logic Devices for Motion Control—A Review. *IEEE Transactions on Industrial Electronics, 54*(1), 559-566. doi:10.1109/tie.2006.885452

Hao R., Cheng Z., and Xiaojie You., (2004), A novel harmonic currents detection method based on rotating d–q reference frame for active power filter. *Proc. of Power Electron. Spec. Conf*., 3034–3038.

Jeraldine A., Viji Albert Victorie., (2014), A comparative study of 3 Phi SAPF with Different reference current generation. *Journal of Control Engineering and Applied Informatics.* 16(4). 99-106.

Jintakosonwit, P., Fujita, H., Akagi, H. (2002). Control and performance of a fully-digital-controlled shunt active filter for installation on a power distribution system.

IEEE Transactions on Power Electronics, 17(1), 132-140. doi:10.1109/63.988679

Juang, C., & Chen, J. (2006). Water bath temperature control by a recurrent fuzzy controller and its FPGA implementation. *IEEE Transactions on Industrial Electronics*, *53*(3), 941-949. doi:10.1109/tie.2006.874260

Khadem, S. K., Basu, M., & Conlon, M. F. (2014). Harmonic power compensation capacity of shunt active power filter and its relationship with design parameters. *IET Power Electronics*, *7*(2), 418-430. doi:10.1049/iet-pel.2013.0098

M. Badoni, A. Singh and B. Singh, "Adaptive Neuro Fuzzy Inference System Least Mean Square Based Control Algorithm for DSTATCOM", IEEE Transactions on Industrial Informatics, pp. 1-1, 2016.

M. Badoni, A. Singh and B. Singh, "Comparative Performance of Wiener Filter and Adaptive Least Mean Square based Control for Power Quality Improvement", IEEE Trans. Ind. Electron., pp. 1-1, 2016.

Monmasson, E., & Cirstea, M. (2007). FPGA Design Methodology for Industrial Control Systems—A Review. *IEEE Transactions on Industrial Electronics*, *54*(4), 1824-1842. doi:10.1109/tie.2007.898281

Muralikrishna, B., Madhumati, G. L., Khan, H., Deepika, K. G. (2014). Reconfigurable edge detection processor using Xilinx Platform Studio. 2014 2nd International Conference on Devices, Circuits and Systems (ICDCS). doi:10.1109/icdcsyst.2014.6926135

Naouar, M., Monmasson, E., Naassani, A., Slama-Belkhodja, I., & Patin, N. (2007). FPGA-Based Current Controllers for AC Machine Drives—A Review. IEEE Transactions on Industrial Electronics, 54(4), 1907-1925. doi:10.1109/tie.2007.898302

Omar, A., Rahim, N., & Mekhilef, S. (2004). Three-Phase Synchronous PWM for Flyback Converter With Power-Factor Correction Using FPGA ASIC Design. *IEEE Transactions on Industrial Electronics*, *51*(1), 96-106. doi:10.1109/tie.2003.822079

Parma, G., & Dinavahi, V. (2007). Real-Time Digital Hardware Simulation of Power Electronics and Drives. *2007 IEEE Power Engineering Society General Meeting*. doi:10.1109/pes.2007.385592

Rodriguez-Andina, J., Moure, M., & Valdes, M. (2007). Features, Design Tools, and Application Domains of FPGAs. *IEEE Transactions on Industrial Electronics*, 54(4), 1810-1823. doi:10.1109/tie.2007.898279

Sriranjani, R., & Jayalalitha, S, (2017), Design of shunt active filter using iterative method to mitigate the harmonics and reactive power. *ARPN Journal of Engineering and Applied Sciences*, 12(24),

Vinod B., Brislin J., (2017), Finite Control Set based Optimized Model Predictive Current Control of Four-leg Shunt Active Power Filter. *Journal of Control Engineering and Applied Informatics*, 19 (1). 67-76.

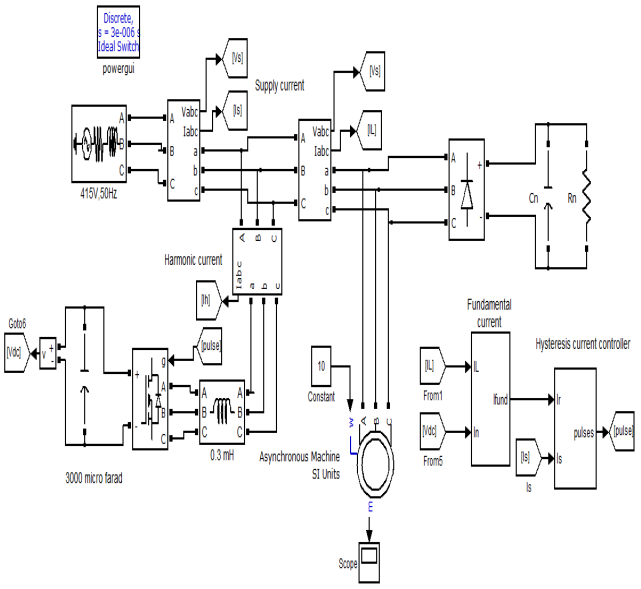
Zeliang Shu, Yuhua Guo and Jisan Lian, "Steady-State and Dynamic Study of Active Power Filter With Efficient FPGA-Based Control Algorithm", IEEE Transaction on Industrial Electronics, Volume. 55, No. 4, pp. 1527-1536, 2008

Zhong. Chen., Dehong Xu., Delay less harmonic detection based on DSP with high-accuracy for active power filter. *Applied Power Electronics Conference and Exposition*, Volume.3, pp. 1817–1823, 2005

Zhuo H. Li, F., Wang Z., Lei W., and Wu L., (2005) A novel time-domain current-detection algorithm for shunt active power filters. IEEE Trans. Power System, 20(2). 644–651.

ANNEXURE – I

Overall system configuration



ANNEXURE – II

System parameters

Parameter	Value
Supply voltage	240 V
Rs, Ls	0.86Ω, 0.01µH
Frequency	50 Hz
Switching frequency	11kHZ
Nonlinear load	30 kW
Linear load	18 kW
Lf	300 µH
Cdc	3000µF
Vdc, ref	800V