A DIGITAL CALIBRATION METHODOLOGY AND ITS APPLICATION TO A HALL SENSOR MICROSYSTEM

M. Pastre, M. Kayal

Electronics Laboratory (LEG)
Ecole Polytechnique Fédérale de Lausanne (EPFL), STI-IMM-LEG
CH-1015 Lausanne, Switzerland

Abstract: *This paper presents a complete digital calibration methodology and its application to the improvement of a Hall sensor-based current measurement microsystem. It is a step-by-step illustration of how generic calibration techniques and circuits can be used on a practical example. First, the methodology is presented. The successive approximations algorithm and its working conditions are detailed. Circuits used for calibration are also discussed, as well as CAD tools useful for integrating background calibration components in electrical simulations. Then, the Hall sensor microsystem is analyzed at system level and its imperfections identified: sensitivity drift and offset drift. The circuit is designed so that for each imperfection to be cancelled, detection and compensation nodes are identified. To these nodes, generic digital calibration circuits are connected to perform continuous background calibration. In the presented current measurement microsystem, the use of the calibration methodology reduced the sensitivity drift down to 50 ppm/°C, which is 10 times less than the state of the art.*

Keywords: *hall sensor, calibration, electrical simulation, methodology.*

1. INTRODUCTION

1.1 Digital Calibration Methodology

This paper shows a case study of the digital calibration methodology proposed in [1] and [2]. This general technique can be applied to all kind of integrated circuits and systems: analog (amplifiers), mixed-signal (ADCs, DACs) and even digital circuits like memories [3][4][5]). Figure 1 presents the application to the offset and noise cancelling ($V_O + V_N$ in the figure) of an amplifier A [6][7][8].

The approach is based on current-mode compensation using sub-binary digital-to-analog converters: A converter (DAC) injects a compensation current in a given node of the circuit, the compensation node (the nulling input Z), where the imperfection can be compensated. The DAC is controlled by a digital algorithm (Ctrl & Successive Approximations Register) that increases or decreases the compensation current. The algorithm bases its decision on the observation of a second node in the circuit, the detection node (here V_{out}), where the sign of the resulting imperfection is sensed by a comparator.

In this way, the algorithm tracks the imperfection and constantly adjusts the compensation current in order to minimize the resulting imperfection.

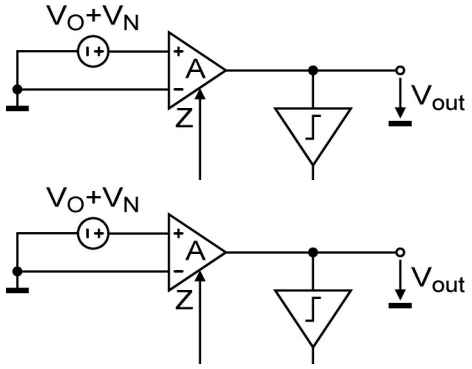


Figure 1. Calibration of the offset of an amplifier

1.2 Hall Sensor-Based Microsystems

The major limitation in Hall sensor-based [9][10] magnetic field and current measurement microsystems is the sensitivity drift. The drift is caused by temperature variations, mechanical stresses and ageing [11][12]. Without calibration, the thermal sensitivity drift is typically 500 ppm/°C with a characteristics as presented in figure 2. Ageing can cause additional drifts of up to 2 %.

With first-order temperature compensation, the thermal drift can be reduced to about 300 ppm/°C. On the other hand, the drift due to ageing is unpredictable and cannot be eliminated without regular calibration. Digital calibration [13][14][15] allows canceling all sources of drift, including purely mechanical stresses and ageing.

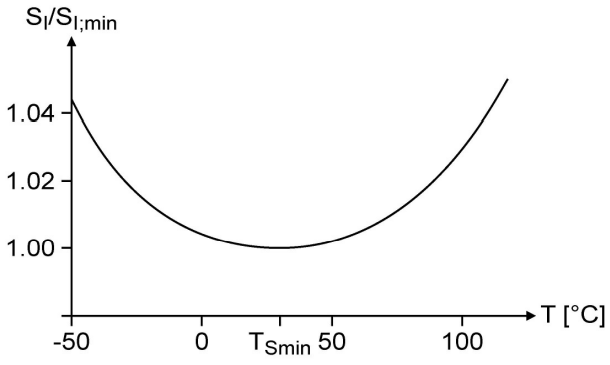


Figure 2. Typical sensitivity drift of a Hall sensor (uncalibrated)

2. CALIBRATION ALGORITHM

2.1 Successive approximations algorithm

The successive approximations algorithm can be advantageously used for calibration because of its simplicity and the flexibility of its working condition. The algorithm performs a dichotomic search over all possible digital control values to identify the best one. For all digital control bits d_1 to d_n (n is the total number of bits of the DAC) and starting by the MSB (Most Significant Bit), it decides whether the bit must be set of not, basing its decision on a simple comparison (C_{out}):

```
reset all di = 0
for i = n downto 1
        set di = 1
        if Cout > 0
                reset di = 0
        end if
end for
```

At the end of the algorithm, the output of the DAC is close to the ideal value. It is not distant from this optimum by more than the weight (w_1) of 1 LSB (Least Significant Bit).

It is noteworthy that the algorithm performs in n steps, which represents only a complexity of $\log_2(FS)$, where the full scale FS is 2^n.

2.2 Working condition of the algorithm

If w_1 to w_n are the weights of the bits 1 to n respectively, the condition for the successive approximations algorithm to work is simply the fact that there must be no missing code:

$$w_i \le w_1 + \sum_{j=1}^{i-1} w_j \ , \ \forall i \in [2..n]$$

If this condition is guaranteed, the successive approximations algorithm will indeed produce a result within 1 LSB to the optimum. In particular, there is no need for the DAC being perfectly linear or having no duplicate codes.

3. CALIBRATION CIRCUITS

3.1 Sub-Binary M/2⁺M DACs

The M/2⁺M DACs can be used advantageously with a successive approximations dichotomy algorithm, since the working condition of the algorithm is guaranteed by design. It is indeed true that if the radix is sub-binary, the output

value w_i of the DAC when only control bit d_i is set is necessarily lower than when the all less significant bits (than i) $d_{i-1}..d_1$ are set.

Sub-binary digital-to-analog converters are advantageous because they can be designed to occupy very low area, even for arbitrarily high resolutions [1][16][17]. They are especially well suited for being used in conjunction with the successive approximations algorithms used for calibration.

The M/2M ladder of figure 3 is a pseudo-resistor [18][19] implementation of the well-known R/2R ladder [20]. In this circuit, each transistor implements a pseudo-resistor of equal value, and the ladder divides the current by 2 in each branch. The bottom-most transistors act by pairs in a complementary way: one as a unit-value pseudo-resistor, the other as an open switch, the role depending on the digital control signals. In this way, each vertical current can be switched.
The M/2$^+$M ladders are variants of the M/2M ladder that are voluntarily made sub-binary by increasing the numbers of transistors in the vertical branches.

Figure 4 presents the schematic of a complete M/3M converter, which is a radix-1.77 ladder. Other variants of M/2$^+$M DACs exist, like the M/2.5M ladder for instance, which is a radix-1.86 converter. The difference between them is mainly the radix, but also the required accuracy of the devices used in the ladder. Indeed, very low-precision transistors are sufficient to guarantee proper working of an M/3M ladder, whereas an M/2M ladder requires perfect components to be functional.

In practice, the M/3M ladder is a good compromise between area and radix. Since the transistors composing it don't need to be precise, they can be almost minimum-sized. The overall area of the ladder thus remains so small that it is comparable to the area of the digital register storing its control value.

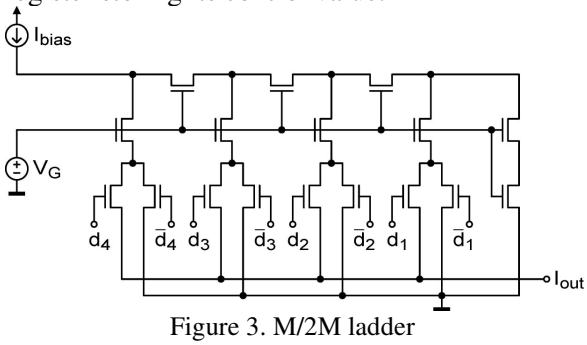


Figure 3. M/2M ladder

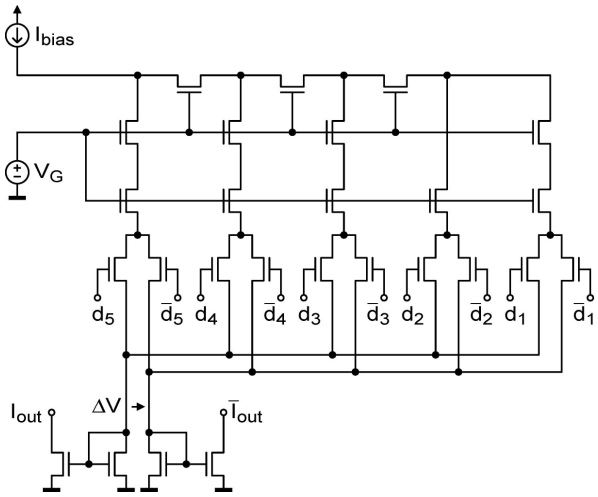


Figure 4. M/3M sub-binary converter

3.2 Step-up/Step-down for continuous-time calibration

The successive approximations algorithm tests each bit of the DAC (starting with the MSB and ending with the LSB) to determine the optimum compensation of the imperfection. This causes the resulting imperfection to be temporarily large during the calibration process, which is not always acceptable. In the current measurement microsystem, this effect is not a problem for the offset cancellation since the latter is removed by demodulation. But the gain correction must remain accurate all the time and the imperfection (gain drift) must be continuously tracked.

The successive approximations algorithm cannot be used directly and a step-up/step-down converter must be used instead. Such a converter can be realized by using two sub-binary DACs connected to the circuit of figure 5. In the configuration presented in the figure, the compensation current is generated by DAC1, whereas DAC2 is adjusted to produce the next compensation current $I_{DAC1} + I_{\varepsilon+}$ if the step is upwards (as in figure), or $I_{DAC1} - I_{\varepsilon-}$ if the step is downwards. The switches S_1 and S_2 are then toggled and the roles of the converters reversed.

This technique allows using the successive approximations algorithm for continuous imperfection tracking, at the cost of a second sub-binary converter. Nevertheless, the overall area of the circuit remains small.

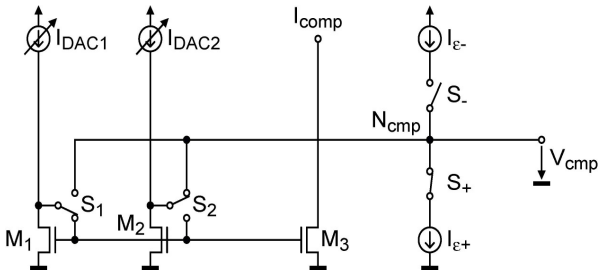


Figure 5. Up/down converter

4. CAD TOOLS

The digital calibration algorithm and the associated calibration circuits can be included in circuit and system design at a very early stage. In fact, their behaviour and interaction with the rest of the circuit can be simulated and the improvement of performance observed.

However, to be done transparently for the user, the simulation process must be slightly adapted. Figure 6 presents how the procedure must be adjusted to include compensation components that, from the designer's point of view, play "automatically" their calibration role. For each user-requested simulation, a pre-simulation is carried out. During this first pass, the simulator identifies the ideal compensation value for each compensation component inserted in the circuit. It then adds a random error corresponding to the quantization error of 1 LSB that the algorithm will reach in practice. Then, the calculated value is used during the second pass where the simulation requested by the user is carried out with a correctly calibrated compensation component.

Figure 7 presents a view of a compensation component in the schematic editor. The decision input for the successive approximations algorithm is derived from the comparison between V_+ and V_-, which are connected to the *detection nodes*. The resolution, full scale and output characteristics of the DAC are specified in the lower part, and the differential current outputs I_{comp+} and I_{comp-} are connected to the *compensation nodes*. Finally, the rest of the circuit can use the Adjust signals to set the correct configuration, depending if the circuit is in calibration mode (first pass), or compensation/normal use mode (second pass).

This simulation method allows seeing the impact of the compensation on system performance. Figure 8 presents the effect of using a compensation component to cancel the offset of an operational amplifier, on the principle presented in figure 1. The statistical dispersions of the offset without and with calibration are presented as the result of Monte Carlo analyses on 1000 samples.

Without compensation, the offset distribution is Gaussian with a standard deviation of about 3 mV. When the compensation is activated, the distribution becomes uniform on a interval reduced by a factor of 240. This value is very close to the resolution of the DAC used in this example, namely 8 bits (256 possible values).

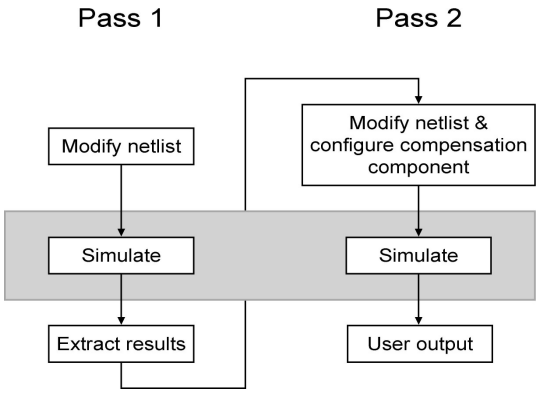


Figure 6. 2-pass simulation process

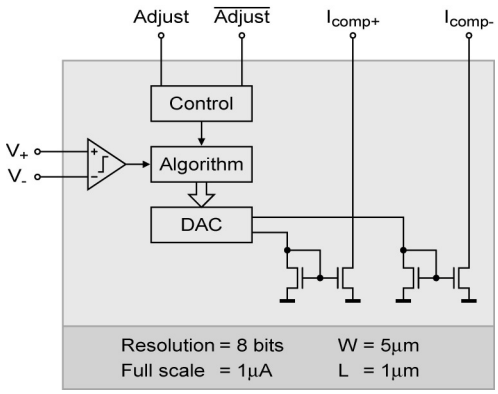
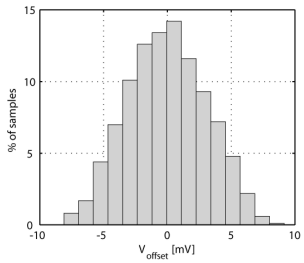


Figure 7. Automatic differential compensation component



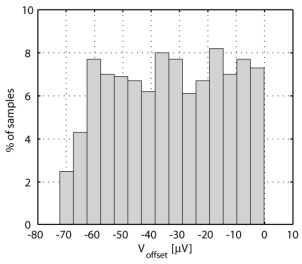


Figure 8. Offset distribution without (left) and with (right) calibration

5. APPLICATION TO THE HALL SENSOR MICROSYSTEM

The first step is to design the system so that detection and compensation nodes can be identified. Figure 9 presents the block diagram of the current measurement microsystem. As in previous implementations, the spinning current technique [21][22] is used to modulate the Hall voltage. An integrated coil [23][24] generates a modulated reference magnetic field, used for sensitivity measurement, at half the spinning current frequency.

The preamplified signal V_{mod} thus consists of 4 successive phases presented in table 1. The table also displays the 3 demodulation schemes that allow to extract in parallel the 3 external (V_{ext}), reference (V_{ref}) and offset (V_{off}) components from V_{mod}. Synchronous switched-capacitor circuits perform the demodulation by implementing the 4 successive arithmetic operations corresponding to each component.

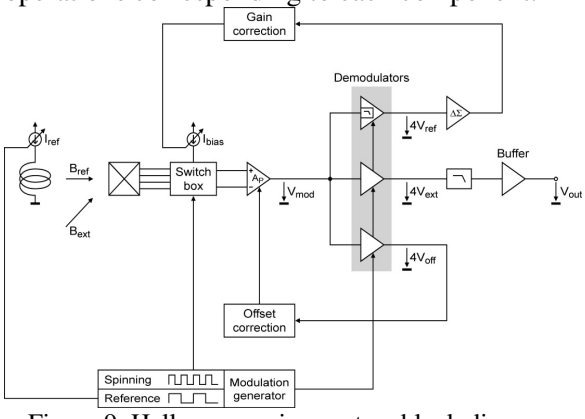


Figure 9. Hall sensor microsystem block diagram

Table 1. Modulation and demodulation schemes

	Modulation			Demodulation		
Phase	Spin.	Coil	V_{mod}	Sig.	Ref.	Off.
1	+	+	$+(V_{ext} + V_{ref}) + V_{off}$	+	+	+
2	-	+	$-(V_{ext} + V_{ref}) + V_{off}$	-	-	+
3	+	-	$+(V_{ext} - V_{ref}) + V_{off}$	+	-	+
4	-	-	$-(V_{ext} - V_{ref}) + V_{off}$	-	+	+
				$4V_{ext}$	$4V_{ref}$	$4V_{off}$

5.1 Sensitivity Calibration Feedback Loop

In this system, the *detection node* for the sensitivity drift is the output of the upper demodulator of figure 9 ($4V_{ref}$), whereas the *compensation node* is the bias current input of the sensor (I_{bias}). Indeed, the preamplifier signal is:

$$V_{mod} = \pm S_I I_{bias} (B_{ext} \pm B_{ref}) + V_{off}, \quad (1)$$

where S_I is the current-related sensitivity of the Hall sensor (which drifts) and I_{bias} its bias current, which is adjusted by the digital algorithm. A diminution of S_I can thus be compensated by an increase of I_{bias}, and conversely. In this way, the global sensitivity of the system, $S_I I_{bias}$, can be made constant by calibration.

Figure 10 shows a more detailed view of the sensitivity calibration feedback loop. The sensitivity measurement is digitized (D_{ref}) by a delta-sigma ADC and compared to a digital nominal value D_{nom}, which represents the desired sensitivity of the system. In this sense, the digital difference δ is the *detection signal*, and the output of the comparator D the *decision signal* for the algorithm. If D is positive, the sensitivity is too high and has to be reduced by decreasing the sensor bias current. If D is negative, I_{bias} has to be increased. The equilibrium is reached when D_{ref} is equal to D_{nom}, and δ is null.

The digital gain correction algorithms controls the $M/2^{+}M$ sub-binary digital-to-analog converter that injects the compensation current I_{comp} in the compensation node N_C. A fixed current source I_{nom} generates the nominal bias current corresponding the targeted sensitivity, and thus I_{comp} accounts only for the drift. This reduces the necessary full scale of the DAC, and thus allows a lower resolution.

The calibration loop adjusts the sensitivity once per second. A long integration time is needed to increase the signal-to-noise ratio since the reference signal level is very low. The 0.1 % of the reference signal, which is the expected calibration resolution, represents only 40 nV at the preamplifier input. This is indeed very close to the white noise floor level of the preamplifier, at 20 nV/√Hz. Nevertheless, the 1 Hz calibration rate still allows tracking all causes of sensitivity variations, including temperature.

The calibration loop can also be disabled temporarily to save power. If the sensitivity variations are slow (with respect to the calibration period of 1 s), the current in the reference coil (a few mA) can be turned off. It is also possible to turn the calibration loop on more often when high sensitivity variations are expected, for instance when fast temperature changes arise.

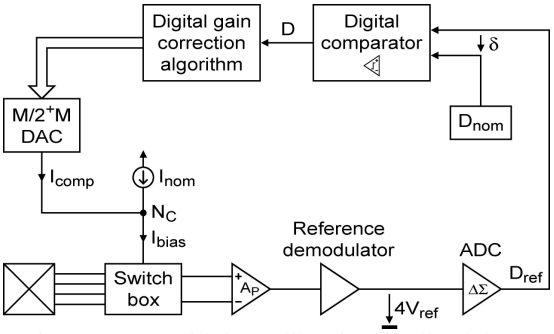


Figure 10. Sensitivity calibration feedback loop

5.2 Offset Calibration Feedback Loop

In the implemented microsystem, the combined offset V_{off} of the sensor and the preamplifier is also corrected. Although this is not necessary since the demodulation schemes cancel the input offset (see table 1), it allows increasing the preamplifier gain, and thus the signal dynamic range. The *detection node* for the offset is the output of the bottom-most demodulator of figure 9 ($4V_{off}$). Figure 11 presents a detailed view of the offset calibration feedback loop. In this case, the voltage in the *detection node* N_D is compared to zero, which is the nominal value for the offset. The sign of the *detection signal* δ is the *decision signal* D for the algorithm. As for the sensitivity calibration loop, the target is $\delta = 0$, and thus the algorithm will null the offset V_{off}.

In this case, the offset is compensated by injecting a compensation current I_{comp} directly in an internal node of the preamplifier. The *compensation node* N_C of figure 11 is implemented in a differential fashion as shown in figure 12, which presents the schematic of the preamplifier.

The compensation currents I_{comp+} and I_{comp-} act differentially and correct the misbalance of the differential pair of the amplifier, but also the offset of the sensor.

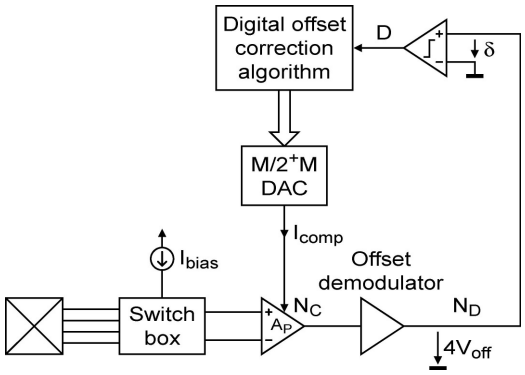


Figure 11. Offset calibration feedback loop

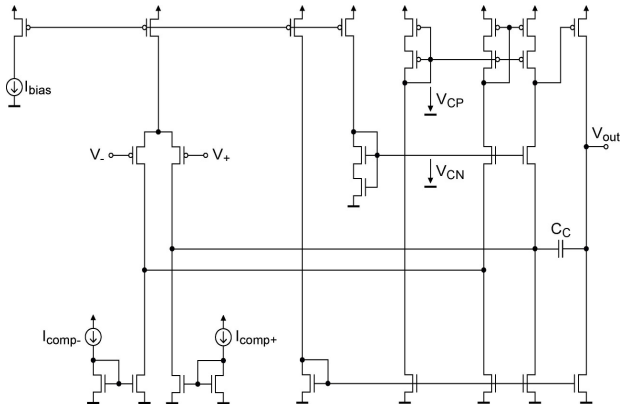


Figure 12. Schematic of the preamplifier

6. SYSTEM IMPLEMENTATION

The complete system of figure 9, including the Hall sensor and the calibration coil, has been integrated in a 0.8 μm process. Figure 13 presents the micrograph of the 11.5 mm^2 circuit.

Figure 14 shows a M/3M DAC with 17 stages, which corresponds to a resolution of 14 bits. It occupies only 0.03 mm^2, and the ladder is smaller than the digital buffer that stores its control value.
Finally, figure 15 shows the step-up/step-down converter allowing the continuous-time calibration. The area of this circuit is 0.015 mm^2 only.

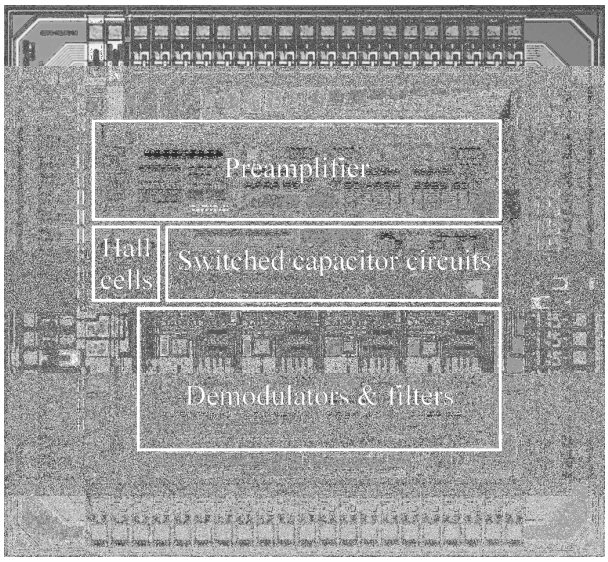


Figure 13. Micrograph of the current measurement microsystem

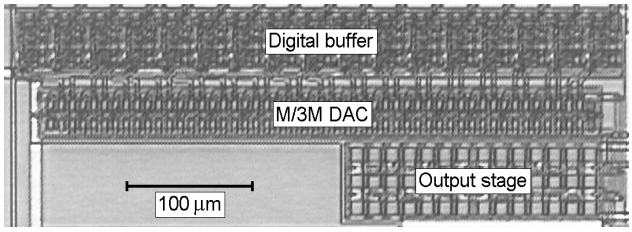


Figure 14. Micrograph of the M/3M sub-binary DAC

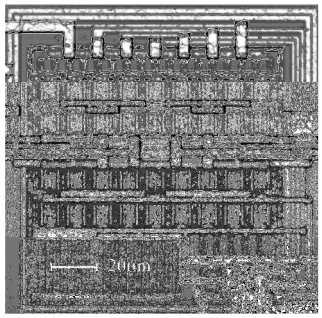


Figure 15. Micrograph of the step-up/step-down converter

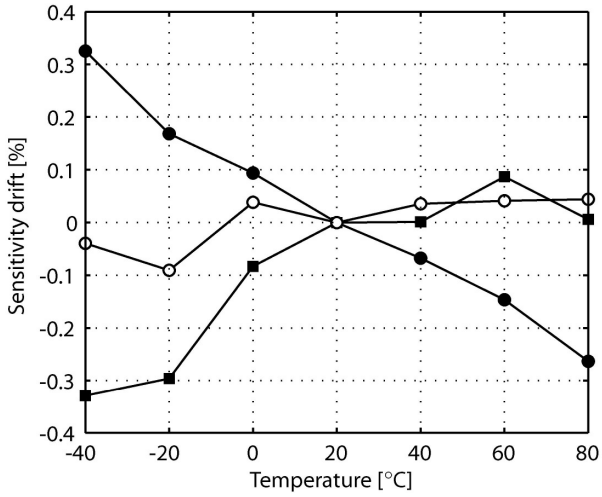


Figure 16. Measured thermal gain drift

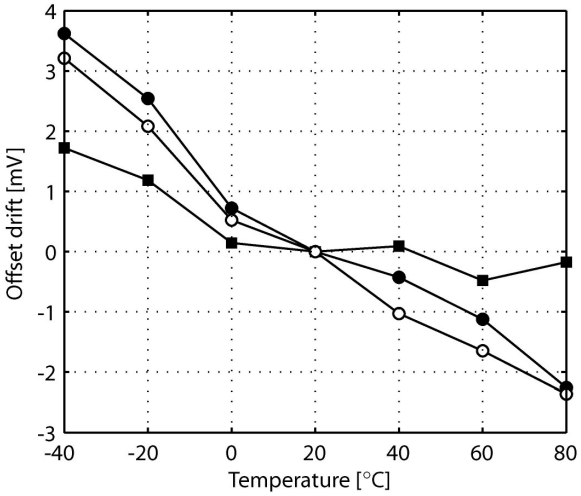


Figure 17. Measured thermal output offset drift

Table 2. Microsystem characteristics

Parameter	Value	Unit
Supply voltage	5	V
Sensitivity	35	V/T
Measurement range	± 50	mT
Bandwidth	500	kHz
Nonlinearity	< 0.1	%
Offset drift	< 50	µV/°C
Gain drift	< 50	ppm/°C

7. MEASUREMENT RESULTS

The gain drift of 3 different samples of the self-calibrated current measurement microsystem as a function of temperature was measured using a fully automatic test setup including a programmable climatic chamber. The results are displayed in figure 16. A mean sensitivity drift of 30 ppm/°C is achieved (with calibration enabled), the worst case being 50 ppm/°C. The calibration reduces the sensitivity drift by a factor 10.

The output offset drift was measured in the same conditions, for temperatures ranging from –40 °C to 80 °C. As displayed in figure 17, the variation is lower than 50 µV/°C.

Another feature of the microsystem is an extended bandwidth of 500 kHz, which is obtained by using a high modulation/demodulation frequency. The sensitivity is 35 V/T, with a full scale of ±50 mT. Table 2 summarizes the characteristics of the microsystem.

8.. CONCLUSION

This paper presents a case study of a complete digital calibration methodology of analog circuits and systems. It shows the complete design flow for detecting, tracking and compensating imperfections, with emphasis on the calibration algorithm and the sub-binary current-mode digital-to-analog converter. It also introduces adapted CAD tools that help designers to simulate circuits including such automatic calibration elements.

This structured methodology can be applied to any system where *detection and compensation nodes* for the imperfection of interest can be identified. By the use of generic compensation circuits, a wide range of imperfections can be tracked and reduced. The additional circuits needed for calibration occupy only a very small area and don't need precise elements to work properly. They thus are a convenient means of improving the performance of analog circuits, and with the evolution of technology towards deep sub-micron, they will become more and more useful. Although the evolution towards digital-friendly technologies rendered analog design more difficult, digital circuits will help counterbalancing this degradation by leveraging analog performance through calibration.

In the proposed application to a Hall sensor microsystem, the use of this automatic calibration approach allowed a reduction by a factor 10 of the gain drift compared to the state of the art.

REFERENCES

[1] M. Pastre, M. Kayal, "Methodology for the Digital Calibration of Analog Circuits and Systems – with Case Studies", Springer, The International Series in Engineering and Computer Science, Vol. 870, ISBN 1-4020-4252-3, 2006

[2] M. Pastre, "Methodology for the Digital Calibration of Analog Circuits and Systems – Application to a Hall Sensor Microsystem", PhD Thesis N° 3210, Ecole Polytechnique Fédérale de Lausanne (EPFL), Lausanne, Switzerland, 2005

[3] M. Blagojevic, M. Kayal, M. Pastre, L. Harik, S. Okhonin, P. Fazan, "Capacitor-Less 1T DRAM Sensing Scheme with Automatic Reference Generation", IEEE Journal of Solid-State Circuits (JSSC), Vol. 41, pp. 1463-1470, June 2006

[4] M. Blagojevic, M. Pastre, M. Kayal, P. Fazan, S. Okhonin, M. Nagoga, M. Declercq, "SOI Capacitor-Less 1-Transistor DRAM Sensing Scheme with Automatic Reference Generation", IEEE Symposium on VLSI Circuits, pp. 182-183, June 2004

[5] M. Kayal, M. Pastre, M. Blagojevic, L. Portmann, M. Declercq, "Reference Current Generator, and Method of Programming, Adjusting and/or Operating Same", EPFL (Switzerland), World patent, N° WO2004102631, November 2004

[6] C. C. Enz, G. C. Temes, "Circuit Techniques for Reducing the Effects of Op-Amp Imperfections: Autozeroing, Correlated Double Sampling, and Chopper Stabilization", Proceedings of the IEEE, Vol. 84, pp. 1584-1614, November 1996

[7] C.-G. Yu, R. L. Geiger, "An Automatic Offset Compensation Scheme with Ping-Pong Control for CMOS Operational Amplifiers", IEEE Journal of Solid-State Circuits, Vol 29, pp. 601-610, May 1994

[8] M. Kayal, R. T. L. Sáez, M. Declercq, "An automatic Offset Compensation Technique Applicable to Existing Operational Amplifier Core Cell", IEEE Custom Integrated Circuits Conference, pp 419-422, May 1998

[9] H. P. Baltes, R. S. Popovic, "Integrated Semiconductor Magnetic Field Sensors", Proceedings of the IEEE, Vol. 74, pp. 1107-1132, August 1986

[10] R. S. Popovic, "Hall Effect Devices", Second Edition, Institute of Physics Publishing, ISBN 0-7503-0855-9, 2004

[11] D. Manic, J. Petr, and R. S. Popovic, "Short and long-term stability problems of Hall plates in plastic packages", Reliability Physics Symposium, pp. 225-230, April 2000

[12] D. Manic, "Drift in Silicon Integrated Sensors and Circuits due to Thermo-Mechanical Stresses", Hartung-Gorre, ISBN 3-9649-591-7, 2000

[13] M. Pastre, M. Kayal, and H. Blanchard, "A Hall Sensor Analog Front End for Current Measurement with Continuous Gain Calibration", IEEE International Solid-State Circuits Conference, pp. 243-243, 596, February 2005

[14] M. Pastre, M. Kayal, and H. Blanchard, "Continuously Calibrated Magnetic Field

Sensor", European Patent Application N° 04405584.6, September 2004

[15]M. Kayal, M. Pastre, "Automatic Calibration of Hall Sensor Microsystems", Elsevier's Microelectronics Journal, Vol. 37, pp. 1569-1575, December 2006

[16]W. G. Bliss, C. E. Seaberg, R. L. Geiger, "A Very Small Sub-Binary Radix DAC for Static Pseudo-Analog High-Precision Memory", Proceedings of the 35th Midwest Symposium on Circuits and Systems, Vol. 1, pp. 425-428, August 1992

[17]G. Scandurra, C. Ciofi, "R-βR Ladder Networks for the Design of High-Accuracy Static Analog Memories", IEEE Transactions on Circuits and Systems, Part I: Fundamental Theory and Applications, Vol. 50, pp. 605-612, May 2003

[18]K. Bult, and G. Geelen, "An inherently linear and compact MOST-only current-division technique", IEEE Journal of Solid-State Circuits, Vol. 27, pp. 1730-1735, December 1992

[19]E. A. Vittoz, X. Arreguit, "Linear networks based on transistors", Electronics Letters, Vol. 29, pp. 297-299, February 1993

[20]M. P. Kennedy, "On the Robustness of R-2R Ladder DACs", IEEE Transactions on Circuits and Systems, Part I: Fundamental Theory and Applications, Vol. 47, pp. 109-116, February 2000

[21]A. Bilotti, G. Monreal, "Chopper-Stabilized Amplifiers with a Trackand-Hold Signal Demodulator", IEEE Transactions on Circuits and Systems, Part I: Fundamental Theory and Applications, Vol. 46, pp. 490-495, April 1999

[22]R. Steiner, C. Maier, M. Mayer, S. Bellekom, H. Baltes, "Influence of Mechanical Stress on the Offset Voltage of Hall Devices Operated with Spinning Current Method", IEEE Journal of Microelectromechanical Systems, Vol. 8, pp. 466-472, December 1999

[23]J. Trontelj, L. Trontelj, R. Opara, A. Pletersek, "CMOS Integrated Magnetic Field Source Used as a Reference in Magnetic Field Sensors on Common Substrate", IEEE Instrumentation and Measurement Technology Conference, Vol. 2, pp. 461-463, May 1994

[24]M. Demierre, "Improvements of CMOS Hall microsystems and application for absolute angular position measurements", PhD thesis N□2844, Ecole Polytechnique Fédérale de Lausanne (EPFL), Lausanne, Switzerland, 2003